Control and stabilization of grid-connected converters operating as constant power load in a Smart Transformer grid scenario

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Control and Stabilization of Grid-connected Converters Operating as Constant Power Load in a Smart Transformer Grid Scenario

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Abstract—The development of power electronics and control technology provides improved performance of the electrical appliances, making them robust to changes in the supply voltage or frequency. However, power electronic converters behave as constant power loads (CPLs), which have negative impedance characteristics, and this non-linear behavior is challenging the stability of the grid. This paper investigates the input impedance of a three-phase low-voltage grid connected ac-dc converter that operating as a CPL when interfaced to a single DC bus and a changeable load. The possibility of adopting a Smart Transformer (ST), a power electronics converter which feeds a low-voltage grid, for the CPL stabilization is also addressed. To analyze the behavior of CPLs, a strategy of impedance modelling is employed. Gain Margin Phase Margin (GMPM) Criterion is referred to judge the stability of the system and verify the stabilization operation for CPLs. Simulation results are presented to be as a support.

Keywords— constant power loads, ac-dc converter, impedance modelling, Smart Transformer, stabilization

I. INTRODUCTION

The characteristic of the constant power load (CPL) is that the input voltage increases when the input current decreases and vice versa, and the product of the voltage and current is a constant as shown in Fig. 1.The gradient of the curve, which is the incremental input impedance, is always negative, and this nature has a destabilizing effect on the system [1]. Many examples of the negative impedance instability are given in [2][3][4][5]. When an ac/dc converter is tightly regulated, the DC bus will have a one-to-one voltage-current characteristic, behaving as a constant power load. As power electronics is becoming more widespread, the enormously increasing CPLs with negative incremental impedances can cause serious instability issues in the electric grid [6].
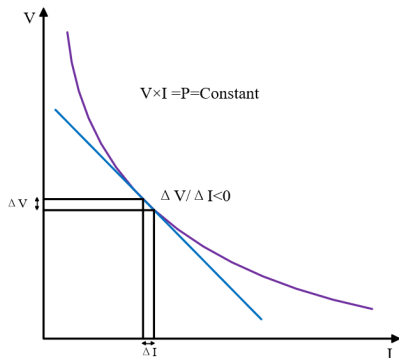

Fig. 1. Constant power loads V-I characteristic

In the smart grid scenario, the idea of upgrading the existing distribution transformers with power electronics has been circulating among researchers [7]. The transformer is also expected to be "smart" to optimally manage the smart grid. The Smart Transformer (ST) is a kind of fully controllable power electronic converter, which can provide advanced services to the grid. The ST can gather information from all the players in the grid and manage the energy flow, improving responsiveness and controllability of the electric grid [8]. Thanks to the increasing controllability, the ST can also be used to modify the grid voltage and potentially stabilize CPLs.

To assess the stability easier, a method of modeling the impedance of system is proposed in [9], which indicates that the characteristic of sources or loads will be effected when some change happens to the structure or parameters of the system.
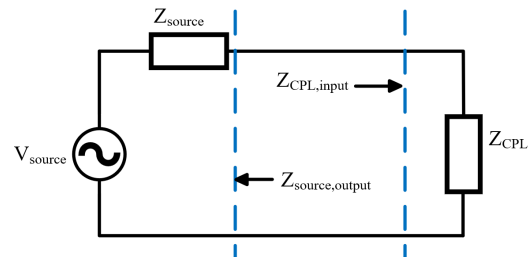

Fig. 2. Equivalent circuit of a CPL included system

Fig. 2 shows the equivalent circuit of a single CPL connected system. The circuit is divided into two individual subsystems. One is the output impedance of the source subsystem Z_{out}. The other is the input impedance of the CPL subsystem Z_{in}. Gain Margin Phase Margin (GMPM) Criterion, a method of evaluating stability, is proposed in [10]. The stability is given as

$$\left| \frac{Z_{out}}{Z_{in}} \right| \leq \frac{1}{GM}, \text{ if not, } |\angle Z_{out} - \angle Z_{in}| \leq 180° - PM \quad (1.1)$$

where GM and PM are expected gain margin and phase margin for a stable system, which are typically GM>1 and PM close to 60 degrees. The gain condition is from the Middlebrook Criterion [11], which conservatively defines the stable region. GMPM Criterion proposes a more flexible condition by considering the phase margin when the gain condition is not satisfied or close to instability.

As tremendously increasing power electronic converters are joining the grid and causing instability, it is necessary to stabilize CPLs. In this paper, a tightly regulated grid-connected three-phase ac-dc converter connected at the low-voltage ac grid is investigated to illustrate the destabilizing effect of CPLs. In Section II, an input impedance model of a three-phase ac-dc rectifier is derived. Section III gives methods of controlling input impedance behavior or output impedance behavior to stabilize the system with a CPL. Section IV describes the control of a smart transformer feeding a Low-Voltage ac grid. Section V shows the simulation results with PLECS software and validated the stabilizing operation with MATLAB software. Section VI summarizes the work and draws the conclusions.

II. IMPEDANCE DERIVING FOR THREE-PHASE AC-DC CONVERTER

In this section, a three-phase ac-dc rectifier operating as a CPL is supposed to be interfaced with a single dc bus and a resistive load. The input impedance of the converter is investigated and derived.

Fig. 3 shows the circuit of a three-phase voltage source converter (VSC), where an LCL structure including filter and grid impedance are considered at the ac side. The dc-link is connected through a capacitor to a resistive load. Applying proportional-integral (PI) controllers and pulse-width modulation (PWM) to switches of the three-phase bridge, the VSC can regulate the voltage of the dc bus at the reference while the load changes.
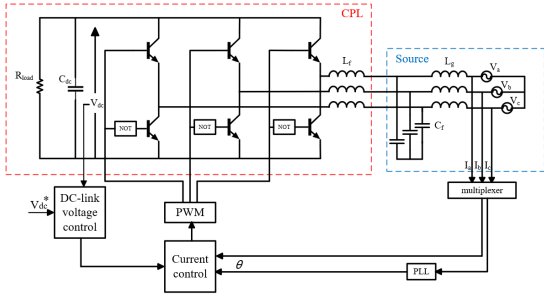

Fig. 3. Circuit and control system of a three-phase ac-dc rectifier

To realize a stable power flow in the system, the grid current should be controlled with a fixed power factor with the grid voltage. Assume that the ac side of the converter is a controlled voltage source. The grid current depends on the voltage difference between the converter and the grid. Therefore, the controller should control the voltage of the converter. The block diagram of current PI controller and the plant is shown in Fig. 4.
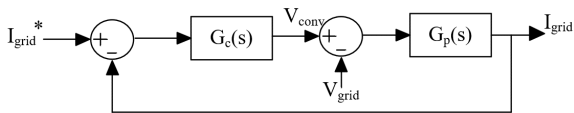

Fig. 4. Current control block scheme

The transfer function of the current plant is the admittance of the LCL structure, which is

$$G_P(s) = \frac{sC_f R_C + 1}{As^3 + Bs^2 + Cs + D} \qquad (2.1)$$

where coefficients in denominator are

$$A = C_f L_f L_g$$
$$B = C_f L_f R_C + C_f L_g R_C + C_f L_f R_g + C_f L_g R_f$$
$$C = L_f + L_g + C_f R_C R_f + C_f R_C R_g + C_f R_f R_g$$
$$D = R_f + R_g$$

The current loop takes the feedback signal of measured grid current, and there should be a zero-order hold for digital implementation, so two PWM delays should be considered, which is given as

$$G_{PWM}(s) = \frac{1}{1 + s/f_s} \qquad (2.2)$$

where f_s is the switching frequency of PWM. Hence, the closed loop transfer function current loop is given as

$$G_{CLTF_{current}}(s) = \frac{G_{C_{current}}(s)G_P(s)G_{PWM}(s)}{1 + G_{C_{current}}(s)G_P(s)G_{PWM}(s)} \qquad (2.3)$$

As Fig. 3 shows, DC-link voltage control is the outer loop of the current loop. The individual block scheme of the voltage loop is shown in Fig. 5. Here $G_C(s)$ is the transfer function of another designed PI controller for voltage control.
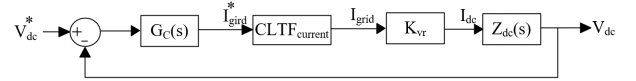

Fig. 5. DC-link voltage control block scheme

Since the current loop outputs the gird current, an approximation of Taylor expansion is required to get the DC-link current. Assume there is no loss in the converter, power transferred from ac side to the dc side can be the same, and it gives

$$I_{dc} = K_{vr} I_g \qquad (2.4)$$

where $K_{vr} = \frac{3V_g}{V_{dc}^*}$ if only the first order component of Taylor expansion is considered. $Z_{dc}(s)$ is the impedance of DC-link the capacitor and the resistive load, which can be obtained as

$$Z_{dc}(s) = \frac{R_{load}}{sC_{dc}R_{load} + 1} \qquad (2.5)$$

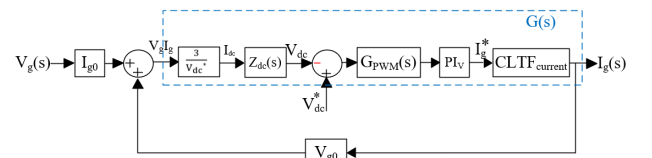One delay of sampling the DC-link voltage should also be considered.

Fig. 6. CPL input impedance block scheme

The input impedance of the CPL can be derived by the block scheme shown in Fig. 6, which is calculated as

$$Z_{in}(s) = \frac{V_g(s)}{I_g(s)} = \frac{1 + G(s)V_{g0}}{-G(s)I_{g0}} \qquad (2.6)$$

where $G(s) = \frac{3}{V_{dc}^*} G_{C_{voltage}}(s) Z_{dc}(s) G_{CLTF_{current}}(s) G_{PWM}(s)$.

The output impedance of the source can be regarded as the parallel of C_f with R_C, and L_g with R_g, which is

$$Z_{out}(s) = \frac{(sL_g+R_g)(\frac{1}{sC_f}+R_C)}{(sL_g+R_g)+(\frac{1}{sC_f}+R_C)} \qquad (2.7)$$

III. STABILIZATION OF CONSTANT POWER LOADS

As mentioned in [6], the trend of research on stabilizing CPLs is always increasing, especially after 2014, during which more than half of related works are published. In this section, two methods are proposed to stabilize the CPL. One is to control DC-link reference voltage adapted to input voltage of the VSC, which should remove the CPL behavior of the VSC itself. The other is to allow the source voltage change with the CPL input voltage, which is possible to be implemented when the source is a fully controlled transformer.

A. Controlling an adaptive DC-link reference voltage
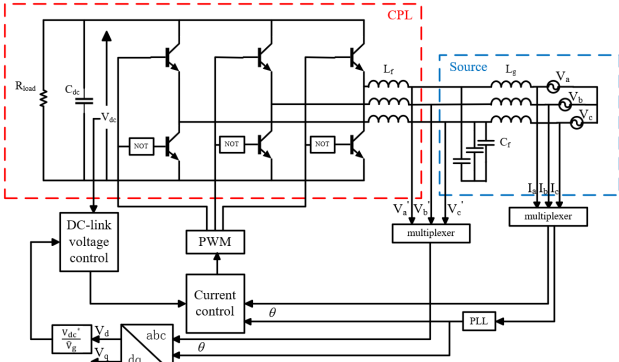

Fig. 7. VSC with an adaptive DC-link voltage reference

Fig. 7 demonstrates the strategy of providing an adaptive DC-link reference voltage, which is implemented by transferring the input voltage from three-phase to d-q frame, and then multiply the d-component with the ratio of the initial DC-link reference voltage and amplitude of grid voltage to become a new DC-link reference voltage. Note that V_a', V_b' and V_c' are the input voltage of the CPL.
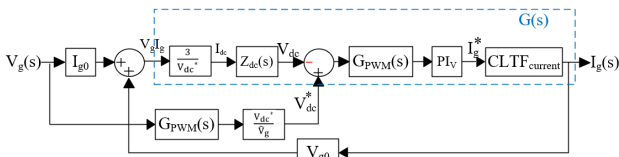

Fig. 8. The block scheme for CPL stabilization with adaptive DC-link voltage reference

A new input impedance block scheme of the VSC is shown in Fig. 8, which is consistent with the circuit and control systems in Fig. 7. Another delay for sampling the input voltage of the VSC is considered the same as (2.2). After simplifying the block scheme, the input impedance of the VSC with adaptive DC-link voltage control is calculated as

$$Z_{in\_adapt}(s) = \frac{1}{(\frac{(V_{dc}{}^*)^2 G_{PWM}(s)}{3Z_{dc}(s)V_{g0}}-I_{g0})(\frac{G(s)}{1+V_{g0}G(s)})} \qquad (3.1)$$

where $G(s) = \frac{3}{V_{dc}{}^*}G_{C_{voltage}}(s)Z_{dc}(s)G_{CLTF_{current}}(s)G_{PWM}(s)$.

B. Implementing control on source output impedance

If a Smart Transformer (ST), which is a fully controllable voltage source, drives the CPL, it is possible to modify the output impedance of the source [12], and potentially stabilize the CPL .

Fig. 9 gives a method of controlling the output impedance of a controlled voltage source, which can be a ST in real world. Here the control strategy is to pull up the source voltage when the required power at the load increases. As the input voltage of the VSC synchronously drops with the DC-link voltage, a controller with a pure gain and resonant control is implemented, which is written as

$$G_C(s) = K_P + K_R \frac{2\xi\omega_0 s}{s^2+2\xi\omega_0 s+\omega_0{}^2} \qquad (3.2)$$

where K_P is the magnitude of the pure gain and K_R is the resonant coefficient. ξ is the damping factor, which is typically 0.7 for a fast and stable system. ω_0 is the desired resonant frequency, which is 100π rad/s here.
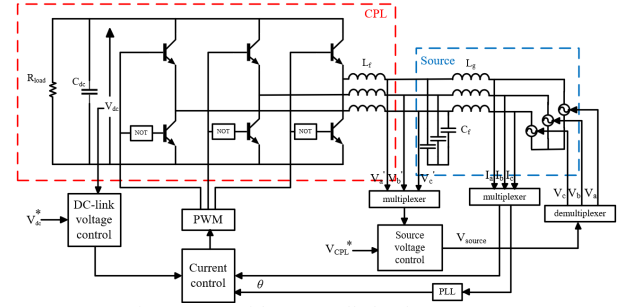

Fig. 9. VSC with a controlled voltage source

The output impedance can be derived by listing the relationship of variables in a simplified circuit and control system as shown in Fig. 10.
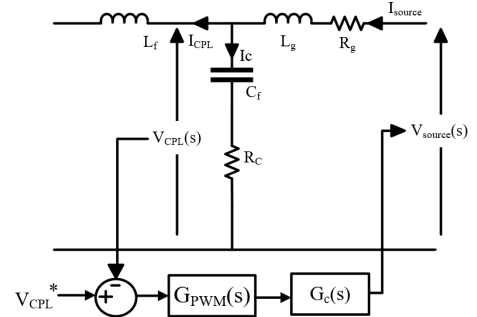

Fig. 10. Simplified circuit and control system for source output impedance calculation

Equations in Fig. 10 are listed as

$$I_{source}(s) = \frac{V_{source}(s)-V_{CPL}(s)}{sL_g+R_g} \qquad (3.3)$$

$$I_{source}(s) = I_{CPL}(s) + I_C(s) \qquad (3.4)$$

$$I_C(s) = \frac{V_{CPL}(s)}{R_C+\frac{1}{sC_f}} \qquad (3.5)$$

$$V_{source}(s) = (V_{CPL}{}^*(s) - V_{CPL}(s))G_{PWM}(s)G_C(s) \qquad (3.6)$$

$$Z_{out}(s) = \frac{V_{CPL}(s)}{I_{CPL}(s)} \qquad (3.7)$$

The output impedance of the source is calculated as

$$Z_{out\_controlled}(s) = -\frac{1}{\frac{1+G_{PWM}(s)G_C(s)}{sL_g+R_g} + \frac{sC_f}{1+sC_fR_C}} \qquad (3.8)$$

IV. MODELING THE LOW-VOLTAGE STAGE OF THE SMART TRANSFORMER

To feed a Low-Voltage (LV) ac grid, a stable output voltage of at the LV stage of the ST must be guaranteed. As shown in Fig. 11, the ST that controls LV dc grid to LV ac grid is operating as a three-phase dc-ac inverter.
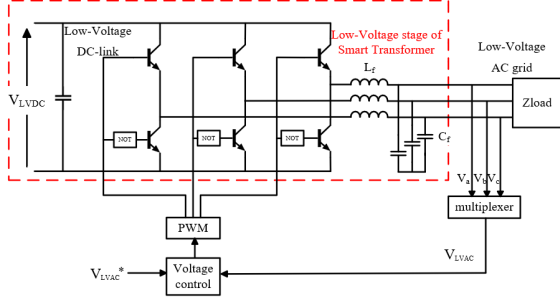

Fig. 11. LV stage of the ST that inverting dc to ac

The voltage controller can be a Type-3 controller, which has an outstanding performance in regulating the output voltage. The controller outputs the required voltage of the inverter, and implement it via PWM. For controller design, the load of LV ac gird should be considered as the worst case, which can be a small impedance with large power factor. Fig. 12 shows the circuit of output filter. The plant transfer function, which is from inverter voltage to output voltage, is calculated as

$$\frac{V_{out}(s)}{V_{inv}(s)} = \frac{Z_{load}}{Z_{load}+R_C} \frac{1+sC_fR_C}{s^2L_fC_f+s\left(\frac{L_f+C_fR_CZ_{load}}{Z_{load}+R_C}\right)+\frac{Z_{load}}{Z_{load}+R_C}} \qquad (4.1)$$
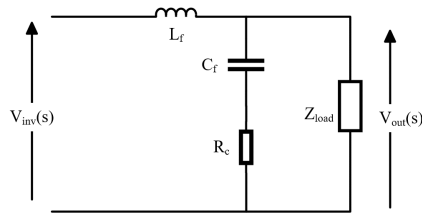

Fig. 12. ST output filter with load

With proper design parameters, the ST should feed the LV ac grid as a controlled voltage source. If the source is fully controllable, it is possible to remove the CPL behavior.

V. SIMULATION RESULTS AND ANALYSIS

In this section, parameters for simulation initialization and simulation results are given. A three-phase ac-dc rectifier shown in Fig. 3 is designed with parameters listed in Table I. In PLECS switching model, the CPL behavior is observed, and the validity of the input impedance model is confirmed in MATLAB. Stability is verified by comparing the derived input impedance of the converter and output impedance of the source. The feasibility of two stabilization operations is checked in both PLECS switching model and MATLAB impedance model.

TABLE I. PARAMETERS OF DESIGNED CONVERTER

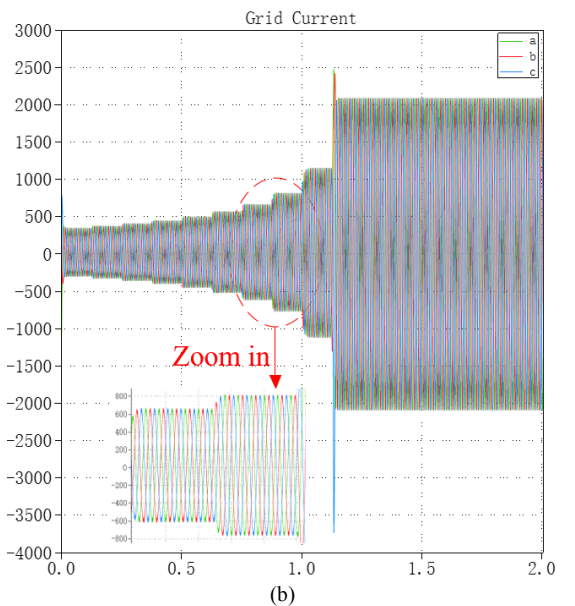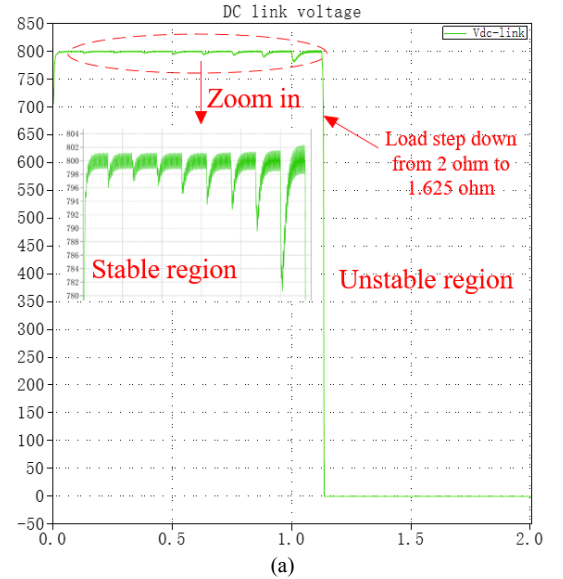| Definition	Symbol	Value
Grid phase voltage (RMS)	V_a,V_b,V_c	230 V
Designed maximum power	P_{max}	640 kW
DC-link voltage	V_{dc}	800 V
DC-link capacitor	C_{dc}	15.9 mF
Switching frequency	f_s	10 kHz
Filter inductance	L_f	215.63 µH
Filter inductor resistance	R_f	0.02 ohm
Filter capacitor	C_f	4.7 µF
Filter capacitor resistance	R_C	0.1 ohm
Source inductance	L_g	100 µH
Source inductor resistance	R_g	0.1 ohm
Test load region	R_{test}	0.1-5 ohm
Current controller	K_{P_C}	1.36
	K_{I_C}	125.66
Voltage controller	K_{P_V}	11.59
	K_{I_V}	728.49

(a)

(b)

Fig. 13. CPL behavior of the grid-connected three-phase ac-dc rectifier (a) DC-link voltage (b) Grid current

Fig. 13 shows how the converter works as a CPL. The test load starts from 5 ohm and steps down 0.375 ohm in every 0.125 seconds. When the load resistance drops, the current increases and the voltage decreases, which is consistent with the V-I curve of constant power load. The small disturbance in the dc voltage can be immediately compensated by the feedback control. The system is stable before 1.125s. After that, the test load steps down from 2 ohm to 1.625 ohm, the DC-link voltage collapses and the converter cannot continue to work, which demonstrates the instability of constant power loads.
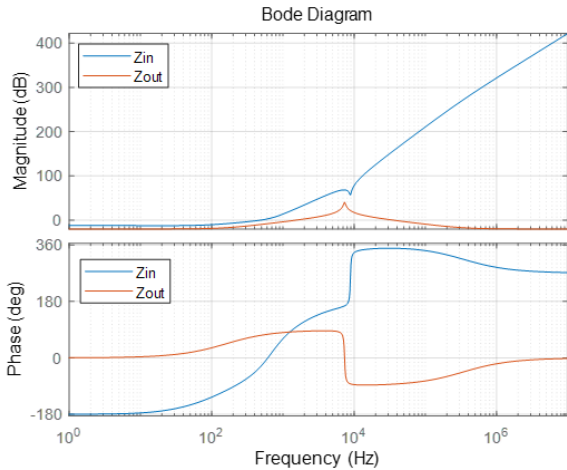

Fig. 14. Impedance model of the VSC

The impedance model of the VSC is plotted in MATLAB as shown in Fig. 14. Phase response of the input impedance, which is around -180 degrees at lower frequencies, shows negative incremental impedance characteristic as a constant power load. According to Fig. 14. the gain condition for stability could be challenged at low frequencies. Hence, an appropriate phase margin needs to be guaranteed. However, the phase difference is obviously larger than the stable boundary. Therefore, the system is unstable from the view of impedance model, which corresponds to the voltage collapse in PLECS switching model.

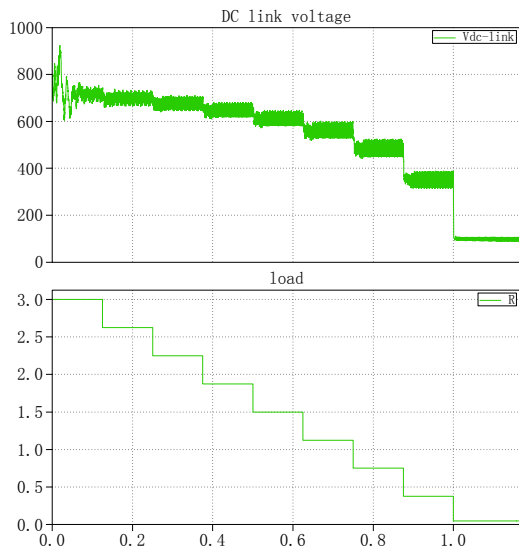*A. Results of modifying input impedance of the VSC*

Fig. 15. Output of the VSC with adaptive DC-link reference voltage

In switching model, the test load starts to step down from 3 ohm. As shown in Fig. 15. With adaptive DC-link reference, the DC-link voltage can be stable with a further smaller resistive load. From the point of view of impedance model, the phase characteristic of the VSC is shifted as shown in Fig. 16, and the phase difference between input impedance and output impedance is significantly minimized, which indicates that the phase criteria for stability is satisfied.
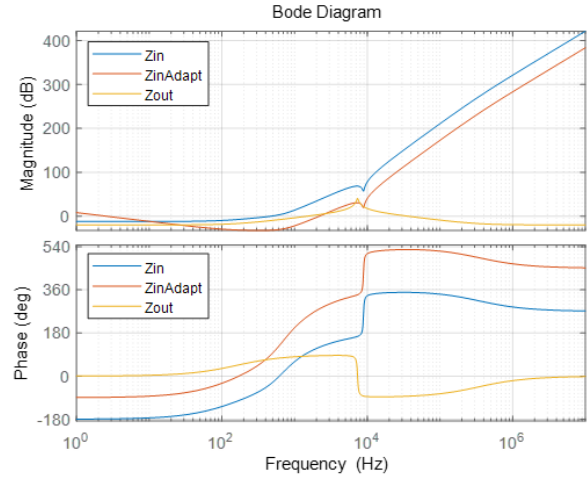

Fig. 16. Impedance model of adaptive control for CPL input impedance

B. Results of modifying the source output impedance

By tuning coefficients in MATLAB and observing the output response, the gain for amplifying the error is supposed to be 0.05, and the resonant coefficient is finally set as 2. In switching model, the load starts to drop down from 2 ohm with 0.2 ohm per step. As shown in Fig. 17, although the dc voltage of the VSC still collapse when the load steps down to 1 ohm, it can work with a load less than 1.6 ohm, which means that the systems allows a higher power. In other words, the stable region is significantly expanded. From impedance model, the phase of the source is shifted as shown in Fig. 18, which minimizes the phase difference between CPL input impedance and source output impedance, confirming the feasibility of this stabilization operation.
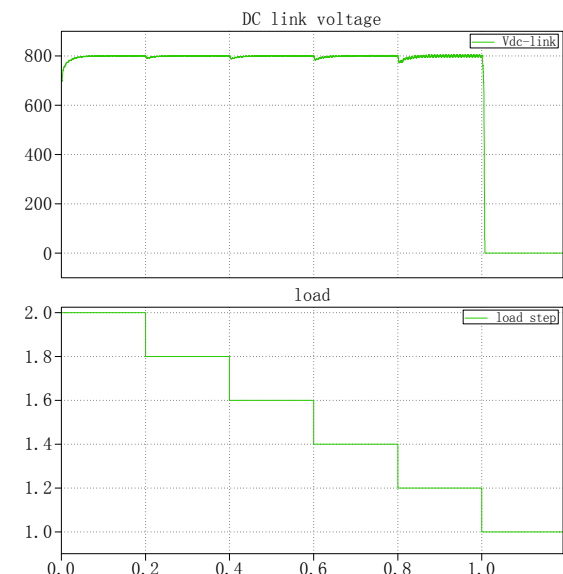

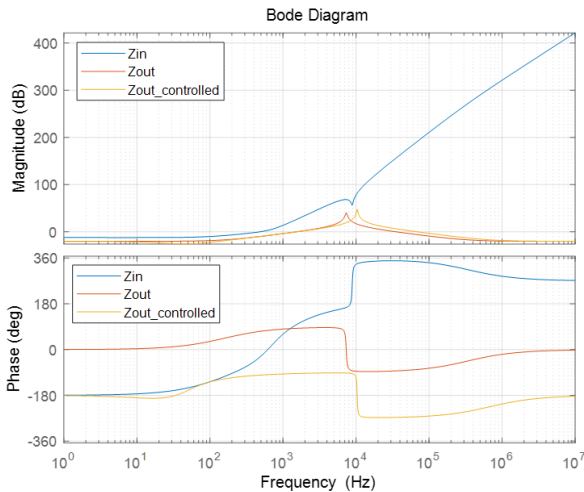Fig. 17. Output of the VSC while controlling the source voltage

Fig. 18. Impedance model of control for source output impedance

VI. Conclusion

This paper has investigated the impedance modeling and stabilization operation for a grid-connected three-phase ac-dc rectifier that operates as a constant power load. The Bode diagram of the CPL input impedance and source output impedance is plotted by using MATLAB. PLECS is used to create the circuit and arrange the time-domain simulation to validate whether the impedance modelling for stabilization of the CPL is correct. The theoretical impedance is validated against switching simulations, and it is matched qualitatively. It can be concluded that the instability of constant power loads is the big phase difference between the input impedance and output impedance. The proposed model can be used to represent the input impedance of the converter. To stabilize the converter, a method of giving adaptive DC-link voltage can shift the phase response of input impedance to meet the stable condition. If the converter is driven by a fully controllable Smart Transformer, it is possible to modify the output impedance to minimize the phase difference. Both two approaches can expand the stable region of the constant power load.

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