<This article has been accepted for publication in a future issue of IEEE Transactions on Power Electronics, but has not been fully edited. Content may change prior to final publication. Manuscript ID:TPEL-Reg-2016-06-1260.R2.>

Wide Input-Voltage Range Boost Three-Level DC-DC Converter with Quasi-Z Source for Fuel Cell Vehicles

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***Abstract*: To solve the problem of the mismatched voltage levels between the dynamic lower voltage of the fuel cell stack and the required constant higher voltage (400V) of the DC link bus of the inverter for fuel cell vehicles, a Boost three-level DC-DC converter with a diode rectification quasi-Z source (BTL-DRqZ) is presented in this paper, based on the conventional flying-capacitor Boost three-level DC-DC converter. The operating principle of a wide range voltage-gain for this topology is discussed according to the effective switching states of the converter and the multi-loop energy communication characteristic of the DRqZ source. The relationship between the quasi-Z source net capacitor voltages, the modulation index and the output voltage, is deduced and then the static and dynamic self-balance principle of the flying-capacitor voltage is presented. Furthermore, a Boost three-level DC-DC converter with a synchronous rectification quasi-Z source (BTL-SRqZ) is additionally proposed to improve the conversion efficiency. Finally, a scale-down 1.2 kW BTL-SRqZ prototype has been created, and the maximum efficiency is improved up to 95.66% by using synchronous rectification. The experimental results validate the feasibility of the proposed topology and the correctness of its operating principles. It is suitable for the fuel cell vehicles.**

***Keywords*: Boost three-level DC-DC converter, fuel cell vehicles, Quasi-Z source, synchronous rectification, wide range of voltage-gain.**

I. Introduction

Non-renewable energy sources continue to be consumed and fossil fuel related emissions continue to increase pollution [1~3]. With regard to transport, the development of clean-energy vehicles can have a major impact on improving air quality (especially in cities) as well as reducing other fossil fuel related problems [4~6]. The fuel cell vehicle is an important type of the clean-energy vehicle and its obvious advantage is that it provides clean propulsion power with zero emission, as well as higher energy utilization [7~9]. However, the fuel cell usually has a current source characteristic with low output voltage and high output current. In addition, it is difficult to use it to supply an inverter to drive a vehicle, due to its soft output characteristic [10~12]. Therefore, it must be interfaced to the DC link bus of the inverter through a step-up DC-DC converter with a wide range of voltage-gain. The wide gap in voltage levels between the fuel cell stack and the DC link bus can be matched, and stable DC link bus voltage can also be obtained.

Usually the conventional Boost two-level DC-DC converter is employed due to its simple structure [13, 14], but, it suffers from disadvantages including limited voltage-gain, and high voltage stress for its power semiconductors. To alleviate the problem of mismatched voltage levels, the rated voltage of the fuel cell stack has to be increased (increasing the difficulty of assembling the fuel cell stack). At the same time, power semiconductors with higher rated blocking voltage need to be employed and consequently the conduction losses can be improved. In order to reduce the high voltage stress of power semiconductors, Boost three-level DC-DC converters have been proposed, and then the voltage stress can be reduced by half [15~17]. However, there remain two essential problems concerning the interface between the fuel cell stack and the DC-link bus, namely the same limited voltage-gain with that of the Boost two-level converter, and the complicate control required for the flying-capacitor voltage balance of the Boost three-level converter, especially the voltage imbalance of the flying-capacitor in the transient state [18] - this latter may cause power semiconductor failure. It is therefore necessary to solve these problems for fuel cell vehicles, which use the Boost three-level DC-DC converter with a flying capacitor.

As to the non-isolated step-up DC-DC converters with high voltage-gain, the voltage multiplier circuits are adopted to extend the voltage-gain [19]. The switched-inductor structures for step-up DC-DC converters can also obtain high voltage-gain, as well as the switched-capacitor DC-DC converters [20, 21]. However, these step-up DC-DC converters with high voltage-gain are too complex to reduce their cost and size. The quadratic Boost DC-DC converter can also achieve a high

Manuscript received June 28, 2016. Accepted for publication November 1, 2016. This work was supported in part by the National Natural Science Foundation of China under Grants 51577130, and 51207104, and in part by the Research Program of Application Foundation and Advanced Technology of Tianjin China under Grant 15JCQNJC03900.

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voltage-gain [22]. However, the power semiconductors of the output side (the high voltage side) suffer from high voltage stresses (due to the high output voltage), and create a high d*v*/d*t* during switching. Although a large conversion ratio interleaved Boost DC-DC converter using two stages in parallel and one series multiplier stage can convert 24V to 200V [23], there still two diodes in the multiplier stage which suffer from the full output voltage stress. A family of diode-coupled-winding Boost DC-DC converters with a high voltage-gain can perform better than their active-clamp counterparts due to recycled leakage energy [24], achieving a maximum efficiency about 91.7%. Based on [23] and [24], a high voltage-gain interleaved Boost DC-DC converter magnetically coupled to a voltage-double circuit was proposed in [25]. In addition, another high voltage-gain Boost DC-DC converter can obtain higher efficiency, which is based on the three-state commutation cell with additional two transformers (six windings) [26].

Z source net has been applied in the traditional step-up DC-DC converters to achieve the higher voltage-gain [27], but their input and output sides don't share the common ground, which may result in maintenance safety and EMI problems. In addition, the output diode can be replaced by an inductor in the Z source DC-DC converters [28], but the voltage-gain is reduced unexpectedly. The diode rectification quasi-Z (DRqZ) source circuit is another modified energy storage circuit structure which has been proposed for the combination of a low voltage DC source and an inverter [29, 30]. It can also be used in the step-up DC-DC converters with the features of lower capacitor voltages and the common ground [31], but its voltage-gain is the same as the conventional Z source DC-DC converters, and the voltage stress of the power switch is still as high as the output voltage. The coupled inductor based Z source DC-DC converters can achieve high voltage-gain by setting the turn ratio of the coupled inductor [32]. However, the spike voltage of the power switches may be very large due to the leakage inductor of the coupled inductor. In [33], a common grounded Z source DC-DC converter with high voltage-gain is presented by changing the connection way of the grounding, the input source and the load are located on the same side of the Z source, instead of being located on both sides of the Z source. It is analyzed in [33] that the voltage stress of the power semiconductors is reduced in the range of half of the output voltage to nearly the output voltage, when increasing the duty cycle (voltage-gain). In addition, the current stress of the power switch is several times as high as the output current while increasing the duty cycle (voltage-gain).

In this paper, a wide input-voltage range Boost three-level DC-DC converter with a diode rectification quasi-Z source (BTL-DRqZ) is proposed as a solution which can reduce the voltage stress of all semiconductors to half of the output voltage; it also has a common ground for the input and output by using the flying-capacitor three-level structure, and operates well with a high voltage-gain, proper duty cycles ($0.5<=d<0.75$), and balancing of the voltage of the flying capacitor without additional hardware. Although one more power switch and diode are employed compared to the conventional quasi-Z source Boost DC-DC converter, the lower rated voltage semiconductors with lower on-resistance can replace the higher rated voltage devices. In addition, the equivalent frequency of the inductor current and the capacitor voltage ripple in the proposed topology is double the switching frequency due to using one additional power switch, diode and flying capacitor, achieved by using the flying-capacitor three-level structure with two phase-shifted 180 degree gate driving signals. These features are beneficial to improve efficiency. In order to improve the efficiency of the proposed converter further, the Boost three-level DC-DC converter with a synchronous rectification quasi-Z source (BTL-SRqZ) is additionally proposed, based on the BTL-DRqZ. This paper is organized as follows: in *Section II*, the topology of the BTL-DRqZ for fuel cell vehicles is presented. The operation principles of the converter topology with a synchronous rectification quasi-Z source are discussed in *Section III*. In *Section IV*, the parameters of all components are designed, and the losses of the proposed topology are analyzed. Then, the experimental results measured from the prototype are analyzed in *Section V*. Finally, the conclusion is delivered in *Section VI*.

II. Topology of DRqZ Source Converter

In order to widen the step-up voltage gain of the Boost DC-DC converter, the DRqZ source net "L_1-L_2-D_1-C_1-C_2" has been investigated. The input of the converter is comprised of the voltage source of the fuel cell $U_{FC}=U_{in}$ and its associated reverse blocking diode D_{FC}. A three-level DC-DC converter with flying-capacitor is adopted, to halve the voltage stress on the power devices and also allow U_{in} and the DC link bus to have a common ground. The resulting BTL-DRqZ for a fuel cell vehicle is shown in Fig. 1.

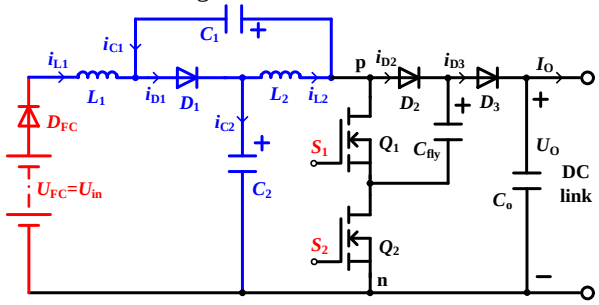


Fig. 1 Proposed Boost three-level DC-DC converter with diode rectification quasi-Z source (BTL-DRqZ) for fuel cell vehicles.

III. Operation Principles

A. Operation states

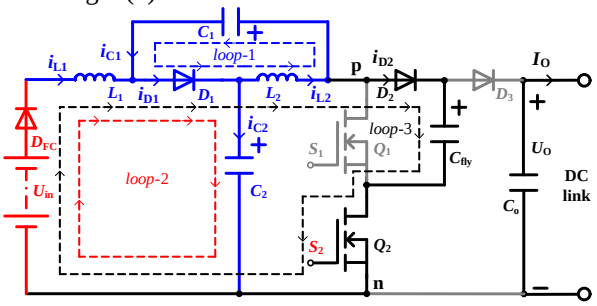
According to Fig. 1, there are four switching states "S_1S_2" in a switching period, i.e. S_1S_2={11, 10, 01, 00}, where "1" represents the power switches Q_1, Q_2 "*ON*", and "0" represents Q_1, Q_2 "*OFF*". L_1 and L_2 are storing energy, while C_1 and C_2 are discharging energy when S_1S_2=11. In the other switching states, L_1 and L_2 discharging energy, whereas C_1 and C_2 are charging. In addition, the sequence of the switching states in a switching period is related to the duty cycle ranges of the power switches Q_1, Q_2. For example, *Sequence I* "01-00-10-00-01" appears within the range of $0<d_1=d_2<0.5$, while *Sequence II* "01-11-10-11-01" can be obtained by the range of $0.5<d_1=d_2<1$, where d_1 and d_2 ($d_1=d_2$) are the corresponding duty cycles for Q_1 and Q_2 in a Boost three-level DC-DC converter. However, the inductors L_1 and L_2 only discharge in *Sequence I*, due to the absence of switching state S_1S_2=11. Therefore, it is likely that

the proposed converter operates within the range of $0.5<d_1=d_2<1$.

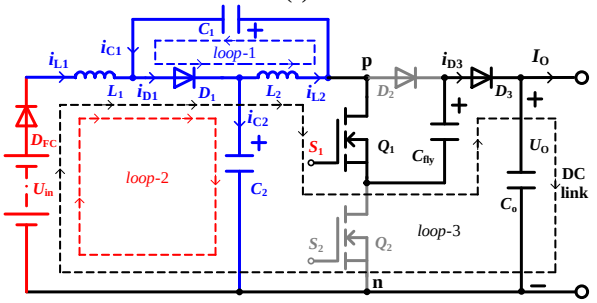
In the active switching states, the energy flow paths between the fuel cell stack source, inductors and capacitors are shown in Fig. 2, and the PWM modulation strategy and important waveforms are illustrated in Fig. 3. In Fig. 2(a), there are three energy flow loops when S_1S_2=01: in *loop*-1, L_2 is discharging, at the same time C_1 is charging through D_1. The inductor current i_{L2} and the capacitor voltage U_{C1} are shown in Fig. 3(e, f); in *loop*-2, L_1 and U_{in} in series are discharging, while C_2 is charging through D_{FC} and D_1. Thus the inductor current i_{L1} and the capacitor voltage U_{C2} can be illustrated in Fig. 3(d, g); in *loop*-3, L_1, L_2 and U_{in} in series are discharging, while the flying-capacitor C_{fly} is charging through D_{FC}, D_1, D_2, and Q_2. Hence the corresponding voltage and current waves are shown in Fig. 3(d, e, h, j, k, m). In addition, the instantaneous PWM voltage of the converter U_{pn} (S_1S_2=01) is simply the voltage across C_{fly}, namely $U_{pn}=U_{Cfly}$, as shown in Fig. 3(n).

When S_1S_2=10, there are also three energy flow paths as shown in Fig. 2(b). It can be seen that the difference between S_1S_2=10 and S_1S_2=01 is the discharging/charging state of the flying-capacitor C_{fly}, e.g. C_{fly}, U_{in}, L_1, and L_2, are in a series connection and discharge to supply the DC link side through D_{FC}, D_1, Q_1 and D_3. The corresponding voltage and current waveforms are shown in Fig. 3(d, e, h, i, l, m). At the same time, the instantaneous PWM voltage of the converter U_{pn} (S_1S_2=10) is described as $U_{pn}=U_O-U_{Cfly}$, rather than the voltage across C_{fly}, as shown in Fig. 3(n).

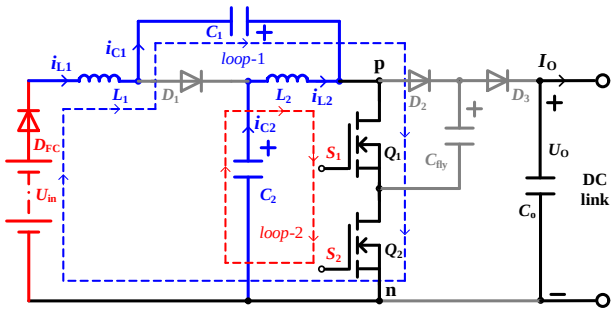
In another active switching state S_1S_2=11, D_1 is OFF due to the reverse voltage of L_1. As a result, two energy flow paths are left, as shown in Fig. 2(c). In *loop*-1, C_1 (which stays in a series connection with U_{in}) is discharging, while L_1 is charging through D_{FC}, Q_1 and Q_2; similarly, C_2 is transferring energy to L_2 through Q_1 and Q_2 in *loop*-2. Consequently, the instantaneous PWM voltage of the converter U_{pn}=0 (S_1S_2=11) can be obtained as shown in Fig. 3(n).



(a)



(b)



(c)

Fig. 2 Energy flow paths among the voltage source, inductors and capacitors in effective switching states. (a) S_1S_2=01 (D_1 is *ON*). (b) S_1S_2=10 (D_1 is *ON*). (c) S_1S_2=11 (D_1 is *OFF*).

B. Operation with wide range of voltage-gain

In order to simplify the explanation, it is assumed the capacitance of the capacitors in Fig. 1 is infinite, as well as the inductance of the inductors. Therefore, capacitors C_1, C_2 are seemed to be constant voltage sources, and L_1, L_2 can be considered as constant current sources. In addition, the flying-capacitor voltage is half of the output voltage U_O, e.g. $U_{Cfly}=U_O/2$. When S_1S_2=01 or S_1S_2=10, L_1 and L_2 are discharging. Thus i_{L1} and i_{L2} are identical in Fig. 2(a, b), and the voltages across L_1 and L_2 are also equal (1):

$$u_{L1\_dis}=u_{L2\_dis} \tag{1}$$

By means of Fig. 2(a, b) and *KVL* (*Kirchhoff's Voltage Laws*), the voltage balance equations can be obtained as follows

$$\begin{cases} U_{in}+u_{L1\_dis}+u_{L2\_dis}=\dfrac{U_O}{2} \\ u_{L2\_dis}=U_{C1} \\ U_{in}+u_{L1\_dis}=U_{C2} \end{cases} \tag{2}$$

When S_1S_2=11, L_1 and L_2 are charging, their voltages u_{L1_ch} and u_{L2_ch} can be described as follows from Fig. 2(c) and *KVL*

$$\begin{cases} U_{in}+U_{C1}=u_{L1\_ch} \\ U_{C2}=u_{L2\_ch} \end{cases} \tag{3}$$

According to (1) and (2), the discharging voltage across L_1 can be written as (4),

$$u_{L1\_dis}=\frac{\frac{U_O}{2}-U_{in}}{2} \tag{4}$$

while the charging voltage of L_1 is obtained by virtue of (2)~(4)

$$u_{L1\_ch}=\frac{\frac{U_O}{2}+U_{in}}{2} \tag{5}$$

Regarding the charging/discharging time of L_1, when S_1S_2=01 and S_1S_2=10, the discharging time t_{L1_dis} of L_1 is described as follows by means of the PWM modulation strategy shown in Fig. 3(a~c)

$$\begin{cases} t_{L1\_dis}=[(1-d_1)+(1-d_2)]\times T \\ d_1=d_2=m=d \end{cases} \tag{6}$$

while the charging time t_{L1_ch} of L_1 is written

$$t_{L1\_ch}=[d_2-(1-d_1)]\times T \tag{7}$$

where $d_1=d_2=d$ are the duty cycles of Q_1 and Q_2 respectively, m is the modulation index, and T is the carrier period.

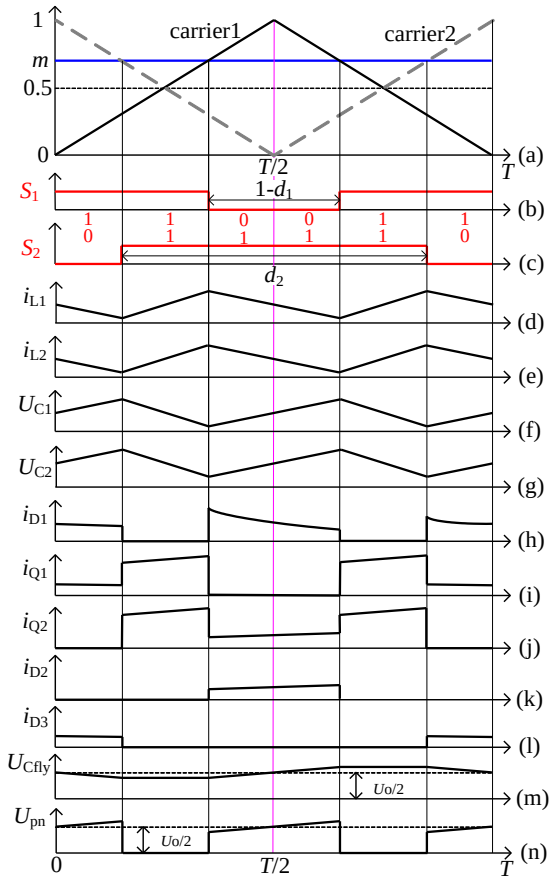


Fig. 3 PWM modulation strategy and important waveforms.

In current continuous mode, the voltage-second balance equation for L_1 can be established as follows, by means of the equal charging and discharging energy in each carrier period

$$u_{\mathrm{L1\_dis}} \times t_{\mathrm{L1\_dis}} = u_{\mathrm{L1\_ch}} \times t_{\mathrm{L1\_ch}} \tag{8}$$

As a result, the step-up voltage-gain M of the BTL-qZ can be obtained by the combination of (4)~(8)

$$M = \frac{U_{\mathrm{O}}}{U_{\mathrm{in}}} = \frac{2}{3-4d} \tag{9}$$

where $0.5 \le d < 0.75$. In addition, the capacitor voltages across C_1 and C_2 can also be gained by virtue of (2), (4) and (9)

$$\begin{cases} U_{\mathrm{C1}} = (d-0.5) \times U_{\mathrm{O}} \\ U_{\mathrm{C2}} = (1-d) \times U_{\mathrm{O}} \end{cases} \tag{10}$$

By means of (9), the proposed topology in Fig. 1 has a wider step-up voltage-gain range, especially the duty cycles of Q_1 and Q_2 are kept within the range of $[0.5, 0.75)$. Consequently, the conventional Boost three-level DC-DC converter's dilemma between the high voltage-gain and the non-extreme duty cycles can be solved by the proposed topology. In Fig. 4, it is shown the comparison of voltage-gain M via duty cycles d among the conventional Boost three-level converter, the interleaved converter in [23], the common ground converter in [33], and the proposed one. Therefore, the proposed converter in Fig. 1 has a wider range of voltage-gain than those previously presented. Even if it operates with lower voltage-gain (i.e. M=2), the more proper duty cycles $[0.5, 0.75)$ will appear, rather than the extreme low duty cycles in [23] and [33].

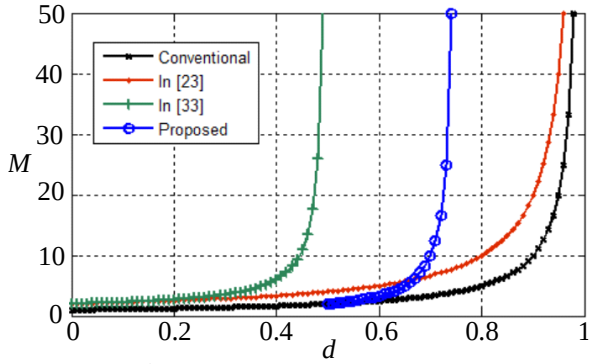


Fig. 4 Comparison of voltage-gain M via duty cycles d among conventional Boost three-level converter, interleaved converter in [23], common ground converter in [33], and proposed one.

C. Self-balance of flying-capacitor voltage

According to Fig. 2(a, b), L_2 is discharging, and its voltage $u_{\mathrm{L2\_dis}}$ is just the voltage across C_1

$$u_{\mathrm{L2\_dis}} \equiv U_{\mathrm{C1}}, \quad (S_1S_2 = 01, \ \ 10) \tag{11}$$

When S_1S_2=01, D_2 and Q_2 are ON as shown in Fig. 2(a), so the flying-capacitor voltage $U_{\mathrm{Cfly\_01}}$ across C_{fly} can be described as follows by (11)

$$U_{\mathrm{Cfly\_01}} \equiv U_{\mathrm{C2}} + U_{\mathrm{C1}} \tag{12}$$

Similarly, when S_1S_2=10, Q_1 and D_3 are ON as shown in Fig. 2(b), the flying-capacitor voltage $U_{\mathrm{Cfly\_10}}$ can also be obtained

$$U_{\mathrm{Cfly\_10}} \equiv U_{\mathrm{O}} - (U_{\mathrm{C2}} + U_{\mathrm{C1}}) \tag{13}$$

While S_1S_2=11, Q_1 and Q_2 are ON, but D_2 and D_3 are OFF as shown in Fig. 2(c). Consequently, the flying-capacitor voltage $U_{\mathrm{Cfly\_11}}$ is maintained. According to (12) and(13), it is concluded the flying-capacitor voltage U_{Cfly} directly depends on the sum of U_{C1} and U_{C2} from the DRqZ source net. Furthermore, the obvious relationship between U_{Cfly} and the output voltage U_{O} is deduced from (10)

$$U_{\mathrm{Cfly}} \equiv \frac{U_{\mathrm{O}}}{2} \tag{14}$$

From the analysis above, it can also be further concluded that the flying-capacitor voltage U_{Cfly} is clamped by the sum of U_{C1} and U_{C2} from the DRqZ source net, and U_{Cfly} can follow half the output voltage U_{O} by this self-balance characteristic, both in the converter's static and dynamic states. Therefore, extra balanced controls for the flying-capacitor voltage can be removed, and the voltage stress of all power semiconductors can still be constant at half the output voltage.

D. Synchronous rectification operation for quasi-Z source

According to (14) and Fig. 2, the voltage stress of the power semiconductors Q_1, Q_2, D_2 and D_3 is half the output voltage. Regarding the voltage stress of D_1 from the DRqZ source system, its blocking voltage is just the sum of U_{C1} and U_{C2} when S_1S_2=11, as shown in Fig. 2(c). Therefore, it is also half the output voltage (10). These advantages above are beneficial to reducing the conduction losses by using appropriate semiconductors, which are of lower on-resistance or lower voltage drop.

The other cause of the conduction losses is the current flowing through the diodes, i.e. D_1~D_3 shown in Fig. 1. The instantaneous currents i_{D1}, i_{D2} through D_1 and D_2 can be described as follows when S_1S_2=01, by means of Fig. 2(a) and *KCL* (*Kirchhoff's Current Laws*).

$$\begin{cases} i_{D1} = i_{L1} + i_{L2} - i_{D2} \\ i_{D2} = i_{L1} - i_{C2} \end{cases}, \quad (S_1S_2 = 01) \tag{15}$$

where $i_{C2}>0$ is the instantaneous current flowing through C_2, i_{L1} and i_{L2} are the instantaneous currents of L_1 and L_2, as shown in Fig. 2(a). Similarly, the instantaneous currents i_{D1} and i_{D3} through D_1 and D_3 can also be written as follows when S_1S_2=10,

$$\begin{cases} i_{D1} = i_{L1} + i_{L2} - i_{D3} \\ i_{D3} = i_{L1} - i_{C2} \end{cases}, \quad (S_1S_2 = 10) \tag{16}$$

whilst D_1~D_3 are OFF when S_1S_2=11. Therefore, when S_1S_2={01, 10}, the relationships of i_{D1}~i_{D3} to i_{L1} can be obtained as follows by means of (15)~(16), the referred relations of $i_{C2}>0$ and $i_{L1}= i_{L2}$

$$\begin{cases} i_{D2} < i_{L1}, & (S_1S_2 = 01) \\ i_{D3} < i_{L1}, & (S_1S_2 = 10) \\ i_{D1} > i_{L1}, & (S_1S_2 = 01,\ \ 10) \end{cases} \tag{17}$$

Consequently, it is concluded that the instantaneous currents flowing D_2, D_3 of the proposed converter are smaller than the corresponding input current of the voltage source. But, the instantaneous current flowing in D_1 from the DRqZ source network is larger than the corresponding input current of the voltage source. As a result, the conduction loss of D_1 must be the largest among D_1~D_3. In addition, D_1 can be replaced by the synchronous rectification MOSFET Q_{SR} (D_{SR} is its anti-parallel body diode), which is of lower on-resistance. This proposed BTL-SRqZ for the fuel cell vehicles is shown in Fig. 5. The voltage stress of Q_{SR} is also half the output voltage as follows when S_1S_2=11

$$U_{QSR} = U_{C1} + U_{C2} = \frac{U_O}{2} \tag{18}$$

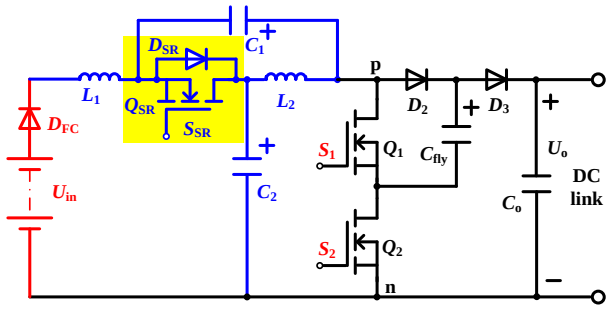


Fig. 5 Proposed Boost three-level DC-DC converter with synchronous rectification quasi-Z source (BTL-SRqZ) for fuel cell vehicles.

As to the gate driving signal S_{SR} for the synchronous rectification power switch Q_{SR}, it can be obtained from "*Exclusive OR*" logic combining S_1 and S_2 depicted in Fig. 6(a~d). In order to avoid conduction behavior of Q_{SR} during the state of S_1S_2=11, the dead time t_d must be added to the ideal gate driving signal of Q_{SR}, by the principle of "*OFF in advance, and ON with delay*" as shown in Fig. 6(b~d). For instance, Q_{SR} must be turned off ahead of time by t_d before the switching state changes to S_1S_2=11, and turned on with delayed time t_d after S_1S_2 is changed to 01 or 10. In addition, t_d is determined by the dead time modulation index m_d and carrier period T easily as follows, shown in Fig. 6(a, d)

$$t_d = m_d \times \frac{T}{2} \tag{19}$$

The anti-parallel body diode D_{SR} conducts when Q_{SR} is turned off in advance, and the current flows through D_{SR} instead of Q_{SR}. As a result, the voltage stress of Q_{SR} is just the forward voltage drop of D_{SR}, i.e. Q_{SR} is turned off with near Zero-Voltage Switching (ZVS), as shown in Fig. 6(d~f). Similarly, Q_{SR} is turned on with ZVS.

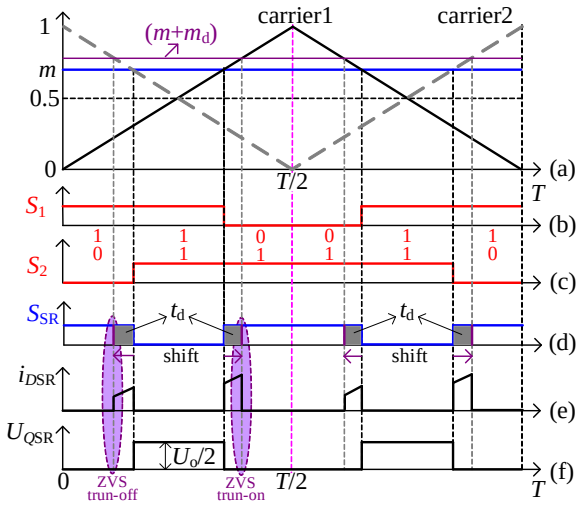


Fig. 6 Gate driving signals of synchronous rectification power switches, dead time and zero-voltage switching.

IV. Component Parameters Design

A. Power switches and diodes

From (10) and (14), it is shown that the voltage U_{Cfly} of the flying capacitor C_{fly} is half of the output voltage U_O, as well as the total voltage of C_1 and C_2. The voltage stress of the power switches and diodes employed in the proposed topology can be deduced in terms of the energy flow paths among the voltage source, inductors and capacitors during their effective switching states as shown in Fig. 2. When S_1S_2=01, Q_1 and D_3 are in the *OFF* state as shown in Fig. 2(a). Therefore, the blocking voltages of Q_1 and D_3 are U_{Cfly} and $(U_O - U_{Cfly})$, respectively. When S_1S_2=10, Q_2 and D_2 are turned off as shown in Fig. 2(b). So, the voltage stresses of Q_2 and D_2 are clamped by $(U_O - U_{Cfly})$ and U_{Cfly}, respectively. When S_1S_2=11, D_1~D_3 are in the *OFF* state as shown in Fig. 2(c). As a result, the blocking voltages of D_1~D_3 are $(U_{C1}+U_{C2})$, U_{Cfly} and $(U_O - U_{Cfly})$, respectively. Stated thus, the voltage stresses of all semiconductors are obtained as follows

$$\begin{cases} U_{Q1} = U_{Cfly} = \dfrac{U_O}{2} \\ U_{Q2} = U_O - U_{Cfly} = \dfrac{U_O}{2} \\ U_{D1} = U_{C1} + U_{C2} = \dfrac{U_O}{2} \\ U_{D2} = U_{Cfly} = \dfrac{U_O}{2} \\ U_{D3} = U_O - U_{Cfly} = \dfrac{U_O}{2} \end{cases} \tag{20}$$

With regard to current stresses (namely average currents in the *ON* state) of the semiconductors Q_1, Q_2, D_1~D_3, they can be obtained as (21), using the ampere-second equations of the capacitors C_{fly} and C_O based on the energy flow paths among the

voltage source, inductors and capacitors in the effective switching states as shown in Fig. 2.

$$\begin{cases} I_{Q1}=\dfrac{4}{3-4d}\times I_O \\ I_{Q2}=\dfrac{4}{3-4d}\times I_O \\ I_{D1}=(\dfrac{4}{3-4d}-\dfrac{1}{1-d})\times I_O \\ I_{D2}=\dfrac{I_O}{1-d} \\ I_{D3}=\dfrac{I_O}{1-d} \end{cases} \tag{21}$$

where I_{Q1}, I_{Q2}, and I_{D1}~I_{D3} are average currents of Q_1, Q_2, and D_1~D_3 when they are in the *ON* state respectively, and I_O is the output load current. In addition, the current stress of D_{FC} is the average current of the inductor L_1, namely

$$I_{DFC}=I_{L1}=\frac{2}{3-4d}I_O \tag{22}$$

It is noted that when S_1S_2=10 and 01, the current stresses of Q_1 and Q_2 are lower, (they are the same as the current stresses of D_3 and D_2 respectively as described in (21)), while they are as high as double the average currents of the inductors i.e. $\dfrac{4}{3-4d}\times I_O$ when S_1S_2=11.

B. Inductors and capacitors

According to the charging and discharging states of the inductors L_1 and L_2 as shown in Fig. 3(b~e), L_1 and L_2 are in the charging state when S_1S_2=11. The inductances of L_1 and L_2 can be deduced as (23)

$$\begin{cases} L_1=(2d-1)\times\dfrac{U_{C1}+U_{in}}{\Delta i_{L1}\times 2f_s} \\ L_2=(2d-1)\times\dfrac{U_{C2}}{\Delta i_{L2}\times 2f_s} \end{cases} \tag{23}$$

where Δi_{L1} and Δi_{L2} are the current fluctuations of L_1 and L_2, and f_s is the switching frequency. Combining (23) with (9) and (10), the inductances of L_1 and L_2 can be obtained as (24), which relates the output voltage U_O, the inductor current fluctuations Δi_{L1} and Δi_{L2}, the switching frequency f_s, and the duty cycle d

$$\begin{cases} L_1=(2d-1)\times(1-d)\times\dfrac{U_O}{\Delta i_{L1}\times 2f_s} \\ L_2=(2d-1)\times(1-d)\times\dfrac{U_O}{\Delta i_{L2}\times 2f_s} \end{cases} \tag{24}$$

When S_1S_2=11, C_1 and C_2 are in the discharging state, the capacitances of C_1 and C_2 can be deduced as (25), in terms of Fig. 2(c) and Fig. 3(b~g)

$$\begin{cases} C_1=\dfrac{(2d-1)\times I_O}{(3-4d)\times\Delta U_{C1}\times f_s} \\ C_2=\dfrac{(2d-1)\times I_O}{(3-4d)\times\Delta U_{C2}\times f_s} \end{cases} \tag{25}$$

where ΔU_{C1} and ΔU_{C2} are the capacitor voltage fluctuations of C_1 and C_2. Regarding the flying capacitor C_{fly}, it is discharged when S_1S_2=10 as shown in Fig. 2(b), and the capacitance of C_{fly} can be obtained as

$$C_{fly}=\frac{I_O}{\Delta U_{Cfly}\times f_s} \tag{26}$$

where ΔU_{Cfly} is the capacitor voltage fluctuation of C_{fly}, that is not related with the duty cycle d of power switches. In terms of Fig. 2(b), the output capacitor C_O is only charged when S_1S_2=10; the capacitance of C_O can be deduced as

$$C_O=\frac{d\times I_O}{\Delta U_O\times f_s} \tag{27}$$

where ΔU_O is the capacitor voltage fluctuation of C_O.

C. Comparisons with other step-up solutions

According to the deduced above, the comparisons can be drawn between the proposed and the other step-up solutions as shown in TABLE I. The conventional Boost and three-level Boost DC-DC converters need one inductor respectively, but their ideal voltage-gain of 1/(1-*d*) is limited due to the effects of parasitic resistance and extreme duty cycles. It is noted that the voltage stress of four semiconductors in the three-level Boost DC-DC converter can be reduced a half comparing with that of the conventional one, due to using two additional semiconductors and one flying capacitor. The high voltage-gain step-up DC-DC converters in [23] and [33] need two inductors respectively. Although six semiconductors are employed in the converter without the snubber circuit in [23], there still exist two diodes with the voltage stress of U_O, and its maximum conversion efficiency is about 92.6%. While a maximum conversion efficiency of the converter in [33] is improved to 94%, three semiconductors and three capacitors are needed. However, the voltage stress of all the semiconductors is between U_O/2 and U_O, e.g. 3U_O/4, rather than U_O/2. Regarding the proposed converter, the number of main components is between those of the converters in [23] and [33], the voltage stress of all the semiconductors is U_O/2, and its maximum conversion efficiency can be 95.66%, which is higher than those in [23] and [33].

V. EXPERIMENTAL RESULTS AND ANALYSIS

In order to verify the feasibility and effectiveness of the proposed BTL-SRqZ for fuel cell vehicles, a scale-down 1.2 kW BTL-SRqZ converter prototype was constructed as shown in Fig. 7. In the experiment, the fuel cell stack source U_{FC}=U_{in} is replaced by an adjustable DC voltage source with a range of U_{in}=60~150V, and the converter voltage loop is controlled by a TMS320F28335 DSP. The power circuit IXTK102N30P MOSFETs (its rated voltage is 300V, and its rated current is 102A, while the output voltage of the converter is U_O=400V), and DSEC60-03A Schottky Barrier Diodes are used. In addition, the switching frequency is f_s=10 kHz, the dead time is t_d=1 μs, the initial values of the qZ source inductors are L_1=228 μH and L_2=225 μH respectively, the load resistor is R_L=133~400 Ω, and the reference output voltage is 400V. The main experimental parameters of the proposed converter are shown in TABLE II.

TABLE I Comparisons between proposed and other step-up solutions.

Step-up Solutions	Voltage Gain	Amount of Semiconductors	Amount of Inductors	Amount of Capacitors	Voltage Stress	Current Stress	Maximum Efficiency
Conventional Boost	$\frac{1}{1-d}$, (0< d <1)	2	1	1	U_O	$\frac{1}{1-d}I_O$	-
Three-level Boost	$\frac{1}{1-d}$, (0< d <1)	4	1	2	$\frac{U_O}{2}$	$\frac{1}{1-d}I_O$	-
Converter without snubber in [23]	$\frac{2}{1-d}$, (0< d <1)	6	2	3	$\frac{U_O}{2}$, U_O	$\frac{1.5}{1-d}I_O$, $\frac{0.5}{1-d}I_O$	92.6%
Converter in [33]	$\frac{2(1-d)}{1-2d}$, (0< d <0.5)	3	2	3	$\frac{U_O}{2(1-d)}$	$\frac{1}{d(1-2d)}I_O$, $\frac{2}{1-2d}I_O$, $\frac{1}{d}I_O$	94%
Proposed converter	$\frac{2}{3-4d}$, (0.5<= d <0.75)	5	2	4	$\frac{U_O}{2}$	$\frac{4}{3-4d}I_O$, $\frac{1}{(3-4d)(1-d)}I_O$, $\frac{1}{1-d}I_O$	95.66%

TABLE II Main experimental parameters of proposed converter.

Parameters and components	Values (units)
Rated power P_n	1.2kW
Input dc voltage U_{in}	60~150V
Output dc voltage U_O	400V
Switching frequency f_s	10kHz
Dead time t_d	1 μs
Inductor L_1	228 μH
Inductor L_2	225 μH
Capacitors C_1, C_2, C_{fly}	450V/660 μF
Capacitor C_O	450V/440 μF
Load R_L	133~400 Ω
MOSFETs Q_1, Q_2, Q_{SR}	IXTK102N30P (300V/102A)
Diodes D_2, D_3, D_{FC}	DSEC60-03A (300V/60A)

Fig. 7 Experimental prototype.

Even when the input voltage is U_{in}=40V, the experimental PWM voltage U_{pn} is shown in Fig. 8, and the frequency of U_{pn} is double of the switching frequency. Although the step-up voltage-gain (U_O/U_{in}) is 10, the actual duty cycles (d=d_1=d_2=1-0.3=0.7) are about 0.7, instead of the actual extreme value of the typical boost converter, which is more than 0.9 under the action of the voltage control loop. Furthermore, the amplitude of U_{pn} is 200V (alternating with the flying-capacitor voltage U_{Cfly} and $U_O - U_{Cfly}$), namely half the output voltage. Thus, it verifies U_{Cfly}=U_O/2 in the steady state, and the flying-capacitor voltage self-balances well without any extra controls.

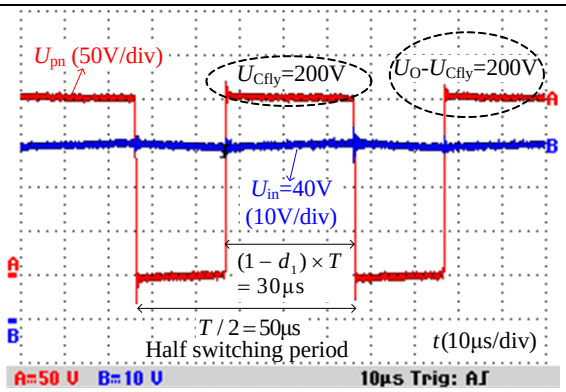


Fig. 8 Output PWM voltage when input voltage U_{in}=40V and M=10.

The experimental results of the synchronous rectification ZVS for the SRqZ source system are shown in Fig. 9. Because of the dead time t_d=1 μs, Q_{SR} is bound to be turned on with a delay, and the anti-parallel body diode D_{SR} is conducted during the dead time. It is noticed that the voltage stress of Q_{SR} changes from the forward voltage drop of D_{SR} to half the output voltage during the dead time. Therefore, Q_{SR} can be turned off with ZVS, as shown in Fig. 9. Similarly, the voltage stress of Q_{SR} changes from half the output voltage to the forward voltage drop of D_{SR} during the dead time. Thus, Q_{SR} can be turned on with ZVS.

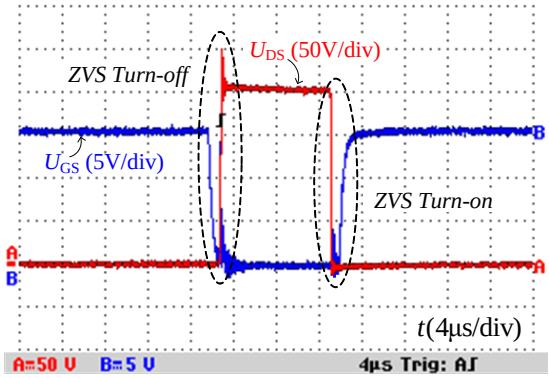
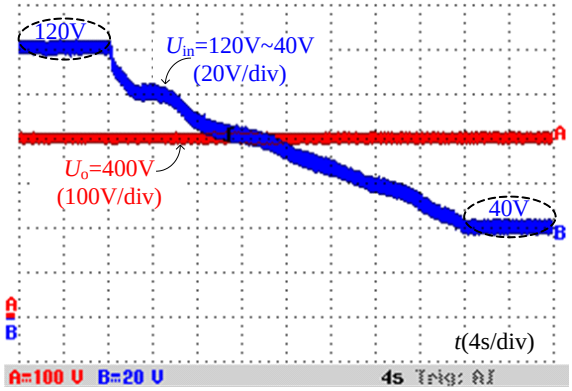


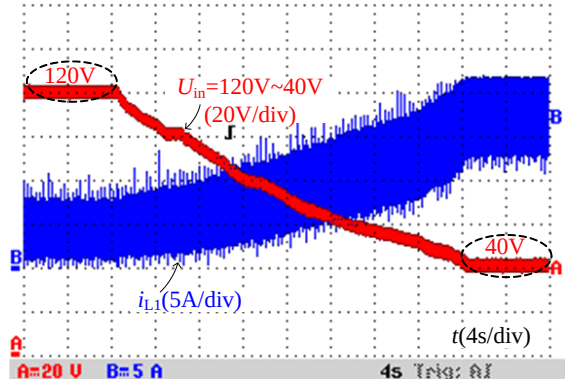
Fig. 9 Experimental results of synchronous rectification ZVS.

As to the applicability of the proposed converter for the fuel

cell vehicles, the experimental results, in which the input voltage U_{in} is changed gradually from the wide range of 120V to 40V over dozens of seconds are shown in Fig. 10(a). It is seen that the output voltage U_O nearly stays around the reference voltage 400V under the action of the voltage control loop, and the wide step-up voltage-gain (U_O/U_{in}) range changes from 3.3 to 10. In fact, the actual voltage-gain in the voltage control loop is more than 3.3 to 10 due to the losses compensation of the converter's operation. Correspondingly, the input current (i_{L1}) increases gradually with the wide-range changed input voltage (from 120V to 40V), as shown in Fig. 10(b), when the load is constant.



(a)



(b)

Fig. 10 Output voltage and inductor current with wide-range changed input voltage from 120V to 40V in dynamic state. (a) Output and input voltages. (b) Input current and voltage.

In Fig. 11, the flying-capacitor voltage U_{Cfly} is changed according to the output voltage U_O (between 200V and 400V in the open loop) in the static and dynamic states. It is noticed that the flying-capacitor voltage U_{Cfly} still keeps at half of the output voltage U_O, especially in the dynamic states *I* and *II*. Because the voltage across the flying-capacitor is clamped by the total voltages of the qZ source capacitors, whose voltages are related to the corresponding real-time duty cycles and the output voltage U_O.

Under the voltage control loop, the proposed BTL-SRqZ converter operates well in conditions of the output voltage U_O=400V, and the output power P_O=1.2 kW. The output PWM voltage U_{pn} and the inductor current i_{L1} are shown in Fig. 12(a). The inductor L_1 is charged when the instantaneous PWM voltage of U_{pn} is zero (S_1S_2=11). Then the inductor L_1 is discharged when U_{pn} stays at $U_O/2$=200V (S_1S_2=01 or 10). In addition, the current i_{L2} of the inductor L_2 is nearly the same as that of L_1, as shown in Fig. 12(b). Therefore, the inductors of the

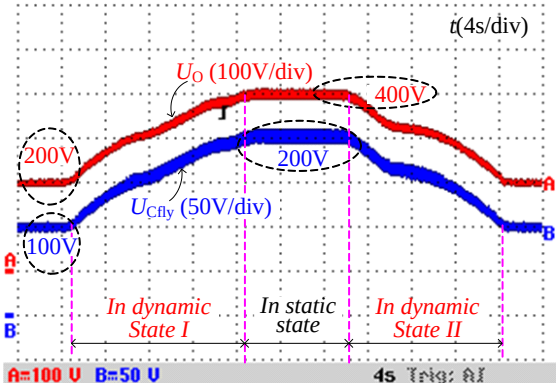
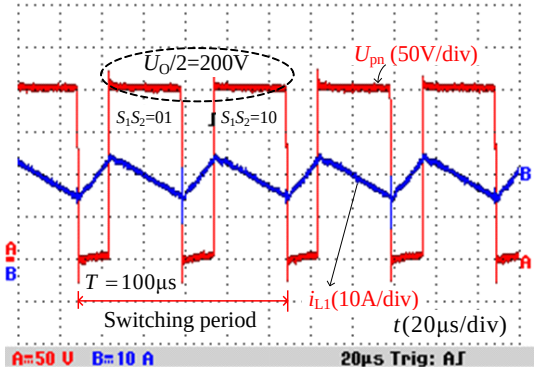
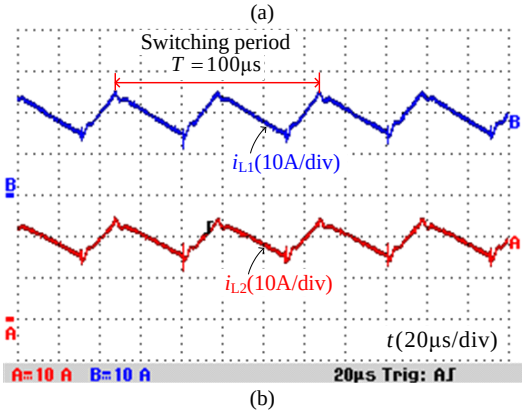


Fig. 11 Dynamic flying capacitor voltage corresponding to the variable output voltage U_O=200~400V in open loop.

qZ source are charged and discharged twice during each switching period. Compared with the converter in [33], there are one additional active power switch and two more diodes in the proposed converter. However, the equivalent switching frequency of the proposed converter is double the one of the converter in [33]. All the volumes of capacitors and inductors in the quasi-Z-source can be reduced by almost a half compared with those of the converter in [33]. In addition, the quasi-Z-source capacitor voltage stresses are lower than those of the converter in [33]. Therefore, the volume of the proposed converter can be significantly reduced compared to that of the converter in [33].



(a)



(b)

Fig. 12 Output PWM voltage and inductor currents. (a) Output PWM voltage and inductor current. (b) Inductor currents.

In order to validate the dynamic behavior of the proposed converter, an experiment was carried out which used a step change of load between 133Ω and 200Ω, and the output voltage and inductor current are shown in Fig. 13. The inductor currents (e.g. i_{L1}) have corresponding responses between 8A and 12A, and the output voltage U_O nearly keeps at constant 400V with

the voltage loop. It can be seen that i_{L1} changes to 12A from 8A over 20ms with the load step-change from 200Ω to 133Ω, and it recovers from 12A to 8A over 20ms with the load step-change from 133Ω to 200Ω.

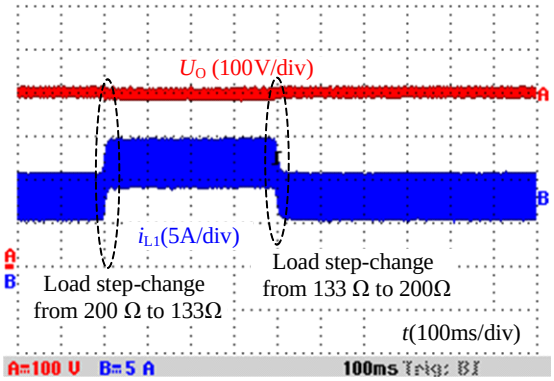


Fig. 13 Output voltage and inductor current when load step-change between 133Ω and 200Ω.

For the wide input-voltage range operation of the proposed converter, the conversion efficiencies related to the variable input voltages (e.g. 60V, 80V, ……, 140V, 150V) and the different output powers (e.g. 400W, 800W, 1200W) are measured by a Power Analyzer (Yokogawa-WT3000). Then, the relationship between the efficiency, the variable input voltages and the different output powers in SR operation are illustrated in Fig. 14. It is noticed that the maximum measured efficiency in SR operation is about 95.66% as shown in Fig. 14. In addition, when the output power is constant and the input voltage declines, the efficiency decreases correspondingly, due to the increasing losses caused by the growing input current. In the same conditions above, the efficiencies in DR operation are also measured, and the SR efficiency is higher than that of DR. The minimum efficiency difference area appears around the medium input voltage (U_{in}=120V), and its average efficiency difference is about 0.6%. While the maximum efficiency difference area exists around the lower and higher input voltage (U_{in}=80V and 150V) areas, and its average value is near 0.85%.

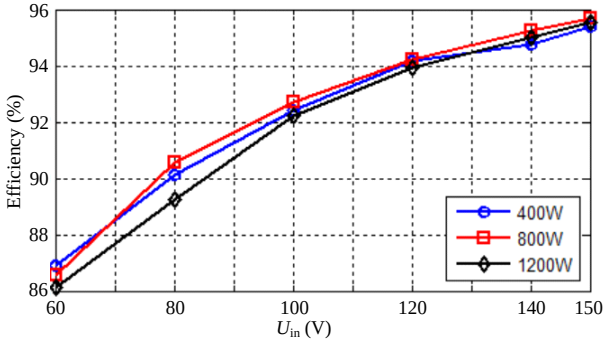


Fig. 14 Relationship between efficiency, variable input voltages and different output powers in SR operation.

The calculated loss distributions for the experiment when U_{in}=150V and P_O=1200W are shown in Fig. 15. In DR operation, the total losses of the converter are 57.06W, and the loss distribution is shown in Fig. 15(a). The turn-on and turn-off (switching) and conduction losses of Q_1 and Q_2 account for 39.87% of the total losses. The conduction losses of all diodes D_1-D_3 and D_{FC} account for 41.57% of the total losses, which is a little more than the switching and conduction losses of Q_1 and Q_2, due to the higher conduction loss of D_1 (in the quasi-Z-source). However, the total losses of the converter are reduced to 49.26W in the SR operation, and the loss distribution is shown in Fig. 15(b). The switching and conduction losses of Q_1 and Q_2 account for 46.19% of the total losses, and the conduction losses of D_2, D_3, D_{FC} and Q_{SR} are reduced to 32.32% of the total losses due to the SR operation of Q_{SR}, instead of D_1 in the quasi-Z-source.

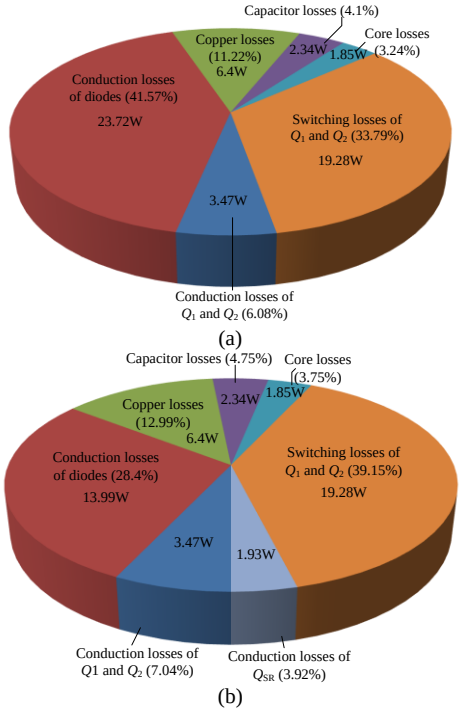


Fig. 15 Calculated loss distributions for experiment when U_{in}=150V and P_O=1200W. (a) In DR operation. (b) In SR operation.

VI. Conclusion

The topology of the BTL-SRqZ is proposed in this paper. It has the advantages of lower voltage stress for the power semiconductors and the common ground between the input and output sides, as well as the wider range of the voltage-gain with modest duty cycles $[0.5, 0.75)$ for the power switches. In addition, the voltage of the flying-capacitor can be clamped well at half the output voltage by the capacitor voltages of the quasi-Z source net in both the static and dynamic states. At the same time, the synchronous rectification power switch operates with ZVS turn-on and turn-off, and the losses of the quasi-Z source circuit can be reduced by the synchronous rectification operation. Therefore, it is suitable to vehicles powered by a fuel cell stack which has a soft output characteristic.

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