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Considerations on the development of an integrated electric inverter for high temperature applications

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Thesis submitted to the University of Nottingham for the degree of Doctor of Philosophy

2022

Abstract

The realization of integrated solutions for electric machine drives is a way to achieve higher space utilization in industrial and transportation electrical power applications. In some cases, limited space affects heat dissipation and the performance of a cooling system, so harsh operating conditions, i.e., high ambient (or cooling) temperature, are a possible additional requirement for integrated drivers. This research investigates in detail the design of some essential or sensitive parts of IMD, highlighting their behaviour under a high-temperature environment. An initial selection of switching power devices is a cornerstone of the inverter design that determines a number of crucial electrical, thermal, and mechanical parameters of the final assembly. Traditionally power modules or custom-designed power devices are the preferable choices for such challenging power electronics applications. An alternative approach based on the parallel connection of discrete MOSFET is underestimated by researchers and is less popular nowadays, although it can offer some valuable advantages. This work presents a comparative analysis of different power devices' packages with a generalized evaluation algorithm focusing on thermal and mechanical aspects in addition to conventional analysis of devices' electrical characteristics. The proposed method helps evaluate the range of feasible power density for PE and the drive itself. The results could give reference figures to demonstrate the capabilities of all popular power packages of novel SiC MOSFETs in the 2-level 3-phase inverter. In selecting power devices, special attention is paid to highlighting possible trade-offs between losses, junction temperature, and occupied volume. Another comparison analysis considers the characteristics of different capacitor materials under various operating conditions and evaluates the required volumetric parameters for DC-link capacitor of the inverter. Several technical challenges related to the adoption and balancing of MOSFET parallel connection are discussed in the thesis. The possible protection of paralleled power devices against the crosstalk effect is studied in detail with a proposed simulation model of the gate driver circuit. Limitation of typical clamping methods if applied to parallel devices is demonstrated. The modified gate driver with a reduced current clamping path generates a lower voltage pulse and enhances the protection against spontaneous turn-on; its efficiency is verified by model simulation and experimentally. New thermal protection for current sensors, providing acceptable conditions up to 130C degrees of ambient temperature, is described and tested.

Acknowledgments

I'm incredibly grateful to my supervisors, Professor Giampaolo Buticchi and Professor Michael Galea, for their guidance, unwavering support, and encouragement in this challenging journey. I would like to express my deepest appreciation to my internal assessor Dr Chunyang Gu for providing technical expertise, sharing her knowledge, and for her great patience. Special thanks to Professor Carlo Cecati for spending his valuable time with me and for his constructive feedback on my work.

I thank my UK supervisor, Professor Pat Wheeler, for his help with thesis improvement and prompt feedback throughout this process. Many thanks to Dr Xiaochen Zhang for his unquestionable support throughout my study and for qualified technical and administrative assistance. I also would like to extend my sincere thanks to Professor He Zhang for developing a supportive team atmosphere and providing an excellent technical environment in the laboratory.

I could not have succeeded in my study without tremendous support from my family, especially my wife, who maintained my spirit and motivation high regardless of any troubles or falls.

List of publications

1. Ahmed Aboelhassan, Yury Mikhaylov, Mukhammed Murataliyev, Ahmed M. Diab, ChungKet Thein, Giovanni Migliazza, Shou Wang, Xiaochen Zhang, Michele Degano, Giampaolo Buticchi, Michael Galea. Design and Implementation of Integrated Motor Drive for High-Speed Aerospace Applications. Under correction.
2. Yury Mikhaylov, Ahmed Aboelhassan, Giampaolo Buticchi, Michael Galea. Considerations on the Development of High-power Density Inverters for highly integrated motor drives. Under correction.
3. Yury Mikhaylov, Giampaolo Buticchi, Paolo Giangrande, Michael Galea, "A gate driver for parallel connected MOSFETs with crosstalk suppression". Submitted to Chinese Journal of Aeronautics. Under Review.
4. Ahmed Aboelhassan, Shuo Wang, Yury Mikhaylov, Giampaolo Buticchi, Michael Galea, and Serhiy Bozhko. A Discontinuous Modulated Model Predictive Control for Low Inductance High-Speed Electric Drive Applications. Working paper

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Chapter 1

Introduction

1.1 Progress of electric transportation

Technical progress and population growth triggered intense emission of greenhouse gases in the second half of 20th century ([1] see Figure 1). Greenhouse gas (GHG), mainly carbon dioxide, is a typical by-product of fuel combustion (according to [2]). Concomitant emission of GHG has a significant long-term harmful effect on the Earth's atmosphere and leads to lifting average temperature[1].

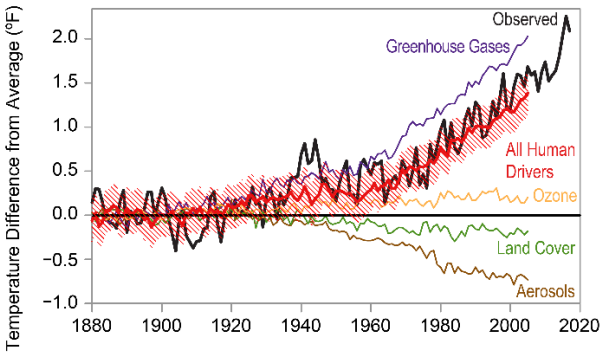


Figure 1 – Increase in global temperature due to natural and human influences[1].

According to the results of climate research (presented in Figure 2), the most optimistic forecast for temperature difference in 80 years is about 1℃ if emissions of CO_2 fall to almost zero level[1]. Without any attempts to address the climate problem, the emissions reach 20Gt/year by 2050, and the temperature rises by 2 ℃ every 50 years (see Figure 2). Therefore, the absence of actions from the society today leads to dramatic consequences later. Considering the inertia in adopting new technological processes by industries, global society has to start applying more sustainable policies as early as possible to prevent irreparable damage.

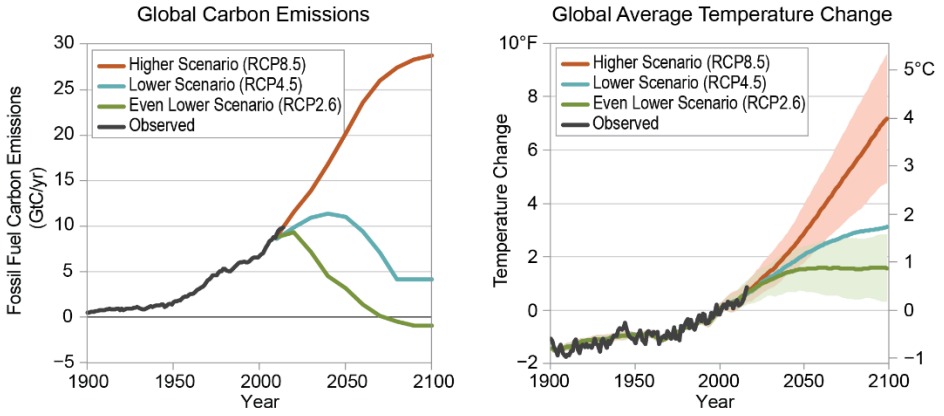


Figure 2 - Observed and projected changes in carbon emissions and temperature[1].

Transportation is the one of serious sources of GHG. For instance, it is responsible for about 18%[3] of pollution over the world and 34% in USA (according to [4], see Figure 3). Therefore, the transition from internal combustion engines of all kinds to fully electric drives becomes an important target for automotive industry on the way to lower CO_2 emissions and more sustainable environment. Together with renewable energy generation, transport electrification is considered one of the prior fields in research of power electronics over the last two decades.

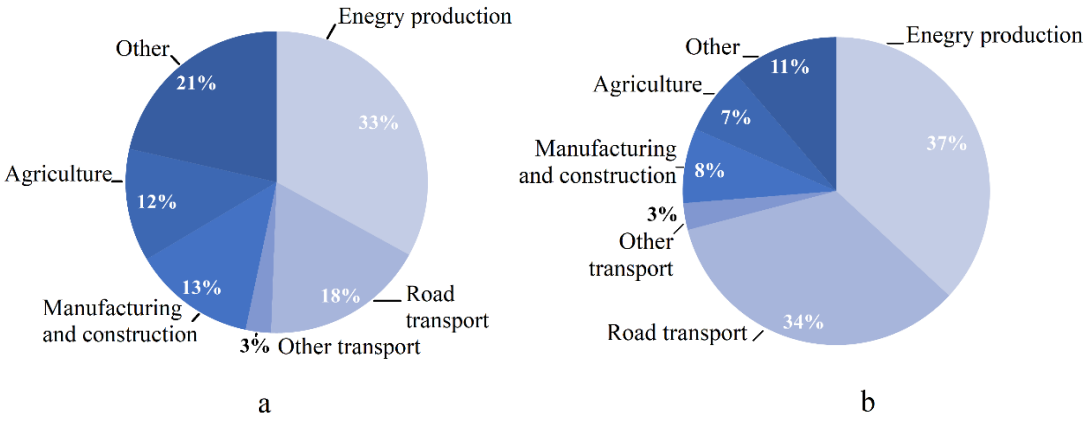


Figure 3 - Total greenhouse gas emissions per sectors of human activity (a – world distribution, b – US distribution).

Continuous development in semiconductor power devices, battery technologies, and electronics miniaturization has contributed significantly to the evolution of all kinds of electric vehicles (hybrids, battery-only, etc.). As a result, the forecasts suggest that EVs occupy the market for up to 60% (or even more if considering the most optimistic Net Zero Scenarios, see Figure 4) in 2035 and almost replace internal combustion vehicles by 2050 [5].

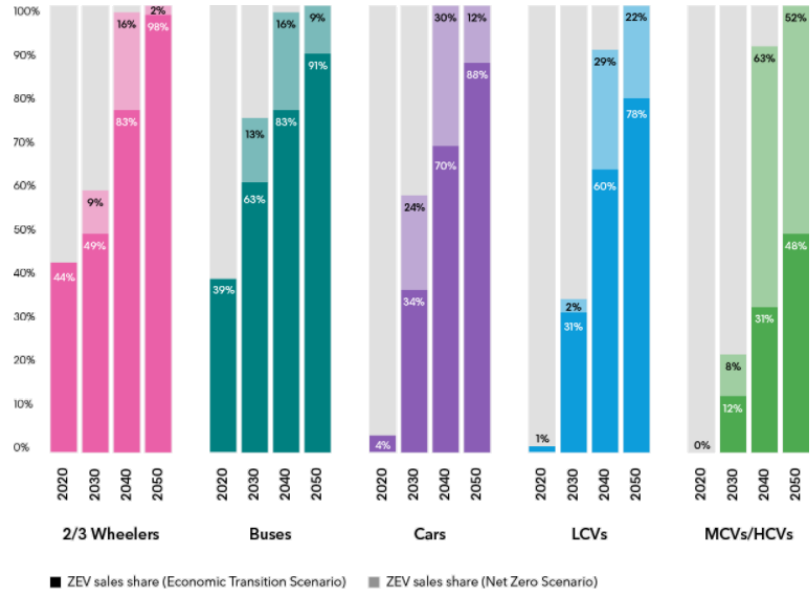


Figure 4 – Forecast for sales share of EVs for period of 2020-2050 [5].

International Energy Agency expects to reduce the total emission of CO_2 generated by transportation from 6 Gt to 0.8 Gt by 2050 (the current level is 3.1 Gt) if the most sustainable scenario occurs (Net zero scenario) [6]. Broad utilization of EV/HEV is responsible for half of that reduction, while the remaining half is expected to come from the increased efficiency of conventional engines and fuel cells (see the forecast for distribution in Figure 5).

The most realistic scenario (solid colour areas in Figure 4) shows that the replacement rate is lower than the optimal value (shaded colour areas in Figure 4), and tremendous efforts from governments and industry are required to make EVs preferable for consumers. Despite the long history, EVs still require government and automotive industry support to become as popular and widespread as ICEV. In [7] the authors study influential factors for EV popularisation in China, including government policy, manufacturer interest, people's education and their awareness of the ecological situation. According to this study, one of the key factors concerning the experts and customers is the technical difficulties with manufacturing and maintenance of EVs (especially battery capacitance and its lifetime). Although the increase in battery capacity and charging rates are considered the most beneficiary technologies to help EVs in their popularization[8], the development of the drive also could provide advantages in terms of efficiency, maintenance requirements, and manufacturing cost. In addition, the creation of new motor drive concepts and designs opens the way to change the conventional representation of road vehicles (for example, the motor-in-wheel structure[9]). Implementing such new concepts is a challenging task as it also requires new designs for traditionally used and trustful systems and components

(power line connections, cooling systems, etc.[10]).

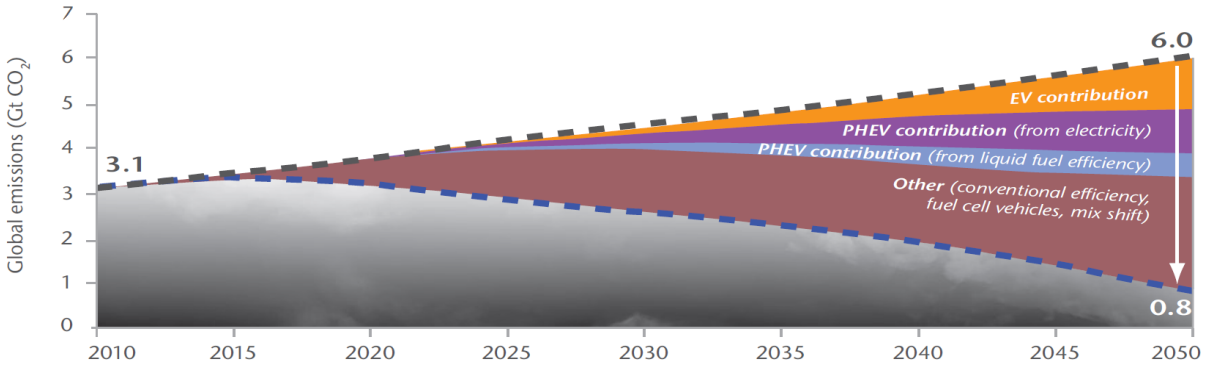


Figure 5 – Forecast of possible reduction in CO_2 global emissions (in transportation) due to development of different EV[6].

Aviation experiences a different situation as its emission is only 1.5-2% of total value due to serious attention to engine efficiency and reduction of fuel consumption. Therefore, replacing the jet propulsion system with the electric one cannot significantly change the amount of air pollution. Moreover, the commercial success of battery-powered aircraft with fully electric propulsion is highly dependent on the achievements in the energy storage density of batteries. Hybrid airplanes are likely to be available in 10-15 years (according to [11], see Figure 6), offering a decent trade-off between reduction of CO_2 emissions and required technological progress. At the same time, total electrification of other airplane systems provides numerous advantages in maintenance cost, mechanical complexity, and flight safety. Avionics, oil, and fuel pumping require direct (by gears) mechanical connection with an engine or a net of high-pressure pipes to operate. With electrical motors, the mechanical power can be generated exactly at the necessary area without the usage of more traditional but less cost-efficient non-electrical methods of power transferring[12].

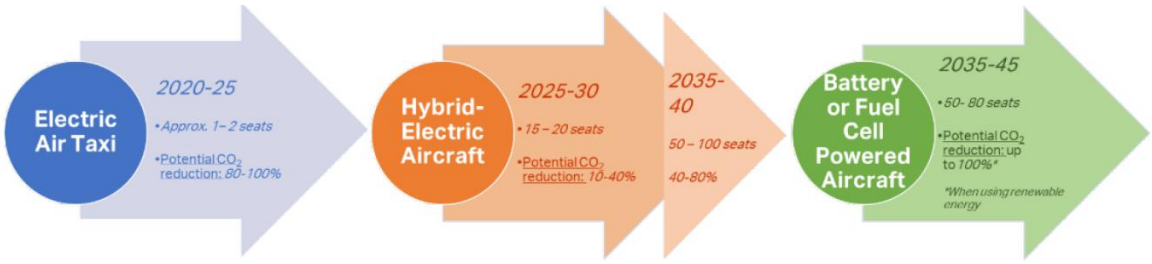


Figure 6 - Step-by-step approach in the penetration of electrically-powered aircraft into the market.

According to the Aircraft Technology Roadmap[11] first fully electrical aircraft enters into service in the next five years. Large passenger aircraft with significant utilization of electrical propulsion systems becomes available only in 2035[11].

1.2 Integration concept in the design of a motor drive.

The rapid spreading of middle-size (personal electrical cars, light airplanes) or small-size (unmanned aerial vehicle, UAV) electrical transport systems raised the problem of space and weight optimization of the powertrain used. Conventional solutions traditionally exploited in the industry or large-size (trains and ships) transportation did not fully satisfy new design requirements. New approaches addressing mass and volume limitation are proposed to increase power densities of power electronics and machines. One of the methods is the integration of a motor and a power converter to achieve better space utilization and reduce the number of housings [13].

An integrated motor drive (IMD) usually includes a motor, an inverter, and a controller that occupy a single enclosure and could be treated as a single unit. Its features could be beneficial at different points of the product lifecycle, and possible pros of the integration approach are summarized in the following list:

Reduction of mass. As mass is a crucial parameter in aviation, the lesser total weight of the housing makes the IMD a preferable candidate to replace traditional mechanical airplane systems.

Reduction of volume. An integrated system occupying less space gives more freedom to achieve desired shapes of the final product or to apply modern design concepts.

Improvement of manufacturing and maintenance. The integrated device is considered a completed and self-efficient entity that the simplifies overall system structure. Single enclosure reduces installation time during the assembling stage and makes logistics for support service during maintenance easier.

The idea of combining both motor and power electronics inside one package was implemented more than 30 years ago in heating, ventilation, and air conditioning (HVAC) applications. However, the number of successful high-power products was quite limited due to their specific features and undeveloped level of power electronic components. Integration was taken seriously into consideration with the development of electrical and hybrid traction systems with motor power levels up to hundreds of kW. For example, the

early generations of EVs (2000 Toyota Prius, Nissan Leaf 2011) often were designed with the classical approach of having separate enclosures for a motor and an inverter connected with thick high-current power cables. From the system structure point of view, high-current cables and connectors are not convenient to use because they are featured bulky sizes and significant weight to maintain the required current without overheating and deterioration of contact quality. With the following modifications, these elements were excluded from powertrains as integration technology was applied (see Figure 7). In addition to the smaller number of enclosures and connection elements, the manufacturer stated a weight reduction of about 10% for the new configuration [14].

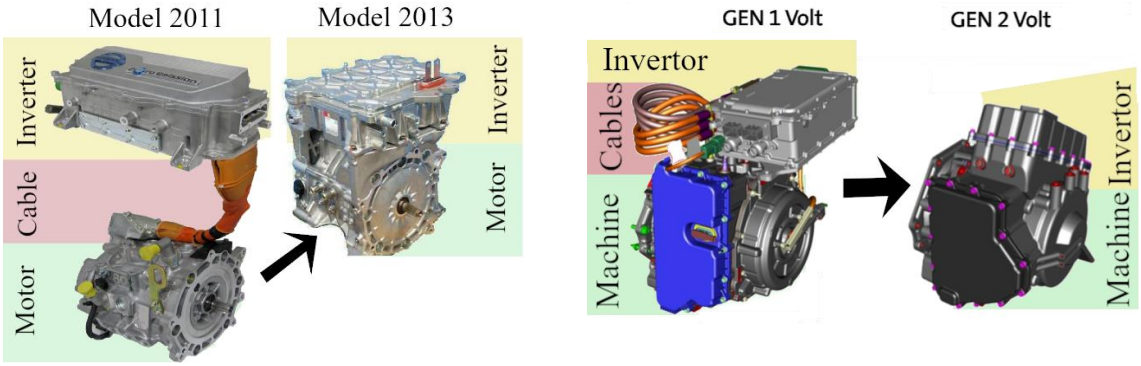


Figure 7 – Adoption of integration approach in commercial EV drive units (left -2011 and 2013 model Nissan Leaf[14], right – Gen 1 and Gen 2 Chevy Volt model[15])

Broad adoption of integrated motor drives in the automotive industry could be considered a success of that approach in achieving better weight and space optimization than traditional concepts. With the development of new car models, engineers try different combinations, shapes, and structures of drive units. For example, Tesla Model S has IMD shaped in 2 cylinders (motor and inverter) with a gearbox between them (see Figure 8). The inverter was designed as a complex prism structure of 3 power modules. The new Tesla Model 3 has a similar motor and gearbox appearance, but the inverter has a classical single-unit configuration though it is built from custom-made components to increase space utilization.

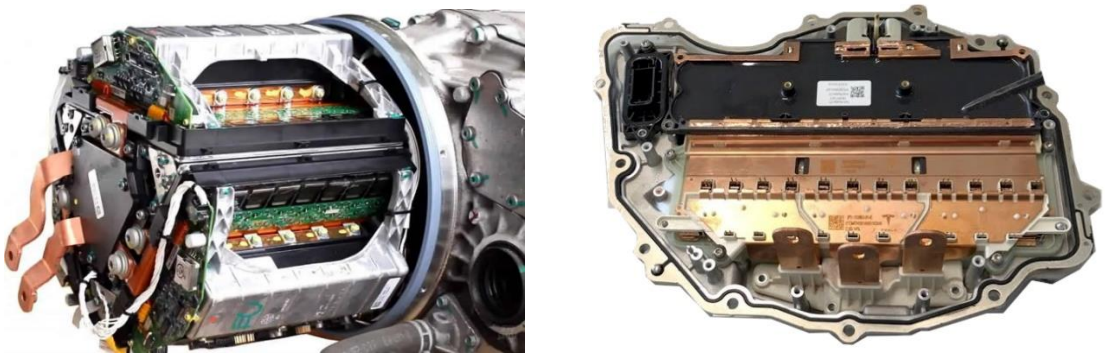


Figure 8 – Examples of commercial integrated inverters demonstrating different structure design (radial 3 boards Tesla Model S - left, flat inverter Tesla Model 3 - right).

Another evidence of significant attention to the progress in this field from researchers and manufacturers is that Advanced Propulsion Centre has included the topic of integrated drives into the list "Industry Challenges 2020-2035+" in the category of Power Electronics[16]. The list consists of research topics that were highlighted by industry representatives, such as:

- The development of lightweight high-efficient drive units, including the usage of advanced material.
- Integration of thermal management for traction systems.
- assembly and disassemble techniques of integrated drives, serviceability.
- Managing noise, vibration, and harshness.
- Advanced control systems for integrated drives.

Integrated motor drives have already passed the stage of purely scientific interest, and their development is beneficial for today's commercial projects and future technologies, aiming for higher sustainability.

1.3 High temperature issues and benefits

Similar to standard electric drives, thermal requirements for IMDs could vary in a wide range depending on the application. However, thermal management of IMD's power electronics is usually more challenging than the one of typical PE due to the influence of EM, limited space, and mechanical complexity of its housing. If harsh environmental conditions are applied together with restrictions on available space or shape of a housing, the design process becomes a problematic multidisciplinary task.

The reasons for the high-temperature operation of IMD could be divided into introduced by the design of PE and external (required by operating conditions).

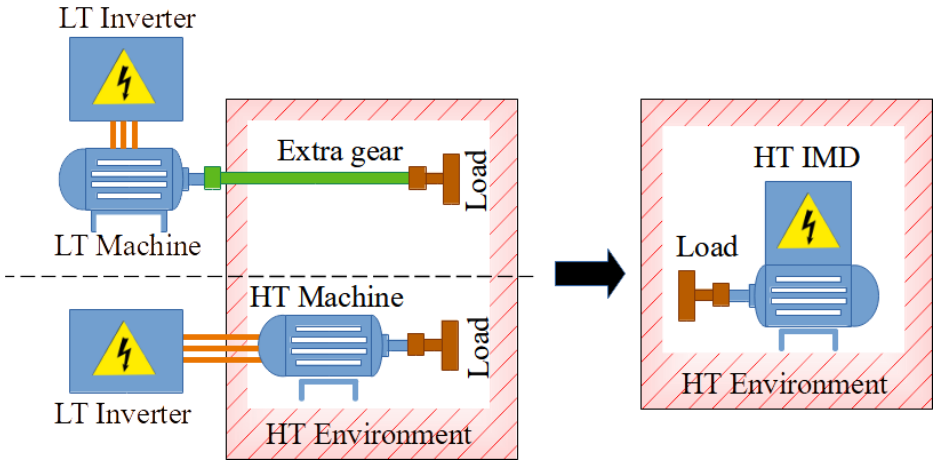


Figure 9 – HT IMD can eliminate additional gears or power cables in case of HT environment.

External (high ambient/coolant temperatures, see Figure 9). Some applications feature high operating temperatures due to fuel burning in vicinity of IMD or excessive heat generation with the lack of cooling. If also applied, the requirements for high gravimetric/volumetric power density could limit the usage of conventional cooling techniques, low-temperature components, and traditional motor drive structures. An excellent example of such an application is any motor drive system near a jet enclosure[17]. The heat generated by the airplane engine creates a high-temperature environment where traditional electronics cannot operate properly (+150°C is the absolute maximum of junction temperature for most Si components). In addition, strict space limitations common for avionics are also a severe obstacle to thermal management or insulation. Hybrid EV also might be equipped with HT IMD to unite cooling loops of a powertrain and an internal combustion engine. The typical maximum temperature of cooling for ICE is about 125°C, and the maximum temperature under the engine hood reaches 120 °C[18]. Usage of HT

coolant for the inverter reduces the overall weight and complexity of the traction system, but it also might decrease reliability and increase cost due to more expensive components. Therefore, trade-off is present, and many factors should be considered with the implementation of HT for automotive applications.

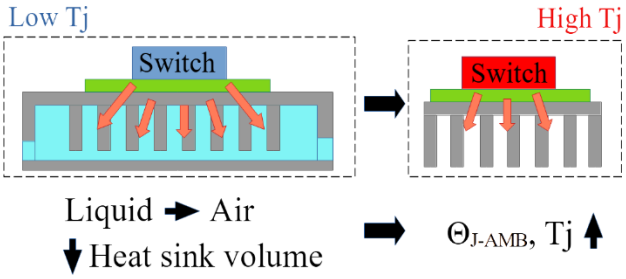


Figure 10 – Smaller heatsink (or the change of cooling type) might save volume in expense of low junction temperature

This method implies the intentional selection of operating point with very high junction temperature in exchange for a smaller/lighter cooling system (or different type of cooling, for example air cooling instead of liquid[19]). This idea might become feasible with the development of new package technologies for advanced semiconductor materials with wide bandgap (such as SiC and GaN) which can operate at very high junction temperatures. The maximum junction temperature of Si power switches does not exceed 175°C. At the same time, specially designed prototypes of SiC switches can work at 300-400°C (with a special HT package and some characteristics limitations)[20]. Unfortunately, most of them are laboratory prototypes and unavailable for purchasing. Today the highest junction temperature of SiC MOSFETs is limited by 200°C for the samples available on the market.

Nevertheless, significant improvements in semiconductors characteristics and relatively high availability of SiC components created acceptable conditions to perform research in the field of HT motor drives and their integrated versions.

1.4 Contribution of this study.

The main target of this work is to analyse crucial points in the design process of HT IMD and propose a generalized approach to its performance evaluation.

In contrast with more specific studies investigating characteristics of a particular HT IMD design, this research focuses on multi-parametric analysis with several types of power devices to highlight their strong and weak points and determine the most influential factors maximizing the output power. The proposed calculation model takes into account the electrical, thermal, and mechanical characteristics of switches, different thermal stacks, and cold plate cooling properties to perform an accurate comparison. The capabilities of parallel connected discrete power switches are studied in the proposed analysis to demonstrate the possible advantages of such structures in high-power traction applications. This work uses components currently presented on the market and available for purchase to exclude any unmatured technologies and solutions that could give a mistaken advantage to either switch type. Moreover, this restriction helps demonstrate the development of SiC industrial manufacturing and the feasible borders of prototypes' power ratings today.

The proposed algorithm analyses PE as a structural part of IMD, considering both PE and EM parameters simultaneously, although typically, in the design process, they are regarded as independent parts of a motor drive. Additional analysis studies required DC link capacitors' dimensions as they might occupy a significant portion of IMD volume and greatly affect total power density.

Further research on HT inverter design has investigated the problem of crosstalk suppression of paralleled MOSFETs which is not addressed in the literature yet. A calculation model that includes the influence of additional parasitic inductance is proposed to assess the amplitude of gate voltage. The simulation demonstrates that the problem becomes more severe with higher junction temperature. The updated design of the gate driver is presented to reduce the influence of the crosstalk and prevent false turn-on of the device.

In order to solve the absence of HT current sensors for HT version of IMD, two methods of maintaining the required temperature environment are proposed in this research. In one method a thermo-electric cooling module is used to cool an external envelope of the low temperature sensor. In the second method, the cooling module acts as an internal heatsink for the hottest parts of the sensor. Thermal models are developed to calculate temperature distribution, power consumption and maximum operating temperature of modified sensors.

1.5 Structure of thesis.

Chapter 2.

The first part of this chapter reviews the state-of-art of integrated motor drives, the most influential technologies, and trends. Special attention is paid to the design, optimization algorithms, and models used to describe motor drive systems. The second part of the chapter is dedicated to the review of HT power electronics and the possibility of applying proposed methods within the integrated motor drive is discussed. Different cooling systems are included in the analysis, and their features are described.

Chapter 3.

This chapter reviews several typical semiconductor power switch devices, and some important characteristics are analysed to indicate the pros and cons of different packages. The typical cases study are explained, and ranges of input parameters are also mentioned. A parametric model of an integrated power inverter with a list of input parameters is described, and the influence of machine parameters is discussed. Volumetric analysis of DC link capacitors is also added to this chapter.

Chapter 4.

The chapter describes the influence of parallel MOSFETs connection on the gate driver circuit and the analysis of the crosstalk mechanism. A simulation model of the injected current is described, and results for different design parameters are presented. The chapter includes special requirements for the modified gate driver and a review of known solutions. One of them is modified to perform with parallel MOSFET, and simulation and experimental testing results are added to the chapter.

Chapter 5.

The chapter includes considerations regarding HT current measurement. HT current sensors are subject to restricted access; novel techniques could help to obtain reliable and accurate current measurements. A review of available traditional methods is presented, and two different cooling methods are proposed to increase the operating temperature range of an off-shelf current sensor. Successful testing of the prototype gives the opportunity to perform measurement with guaranteed accuracy under harsh temperature conditions without using rare components.

Chapter 6.

Conclusion.

The structure of the thesis is explained in Figure 11 with the links between each chapter and additional comments

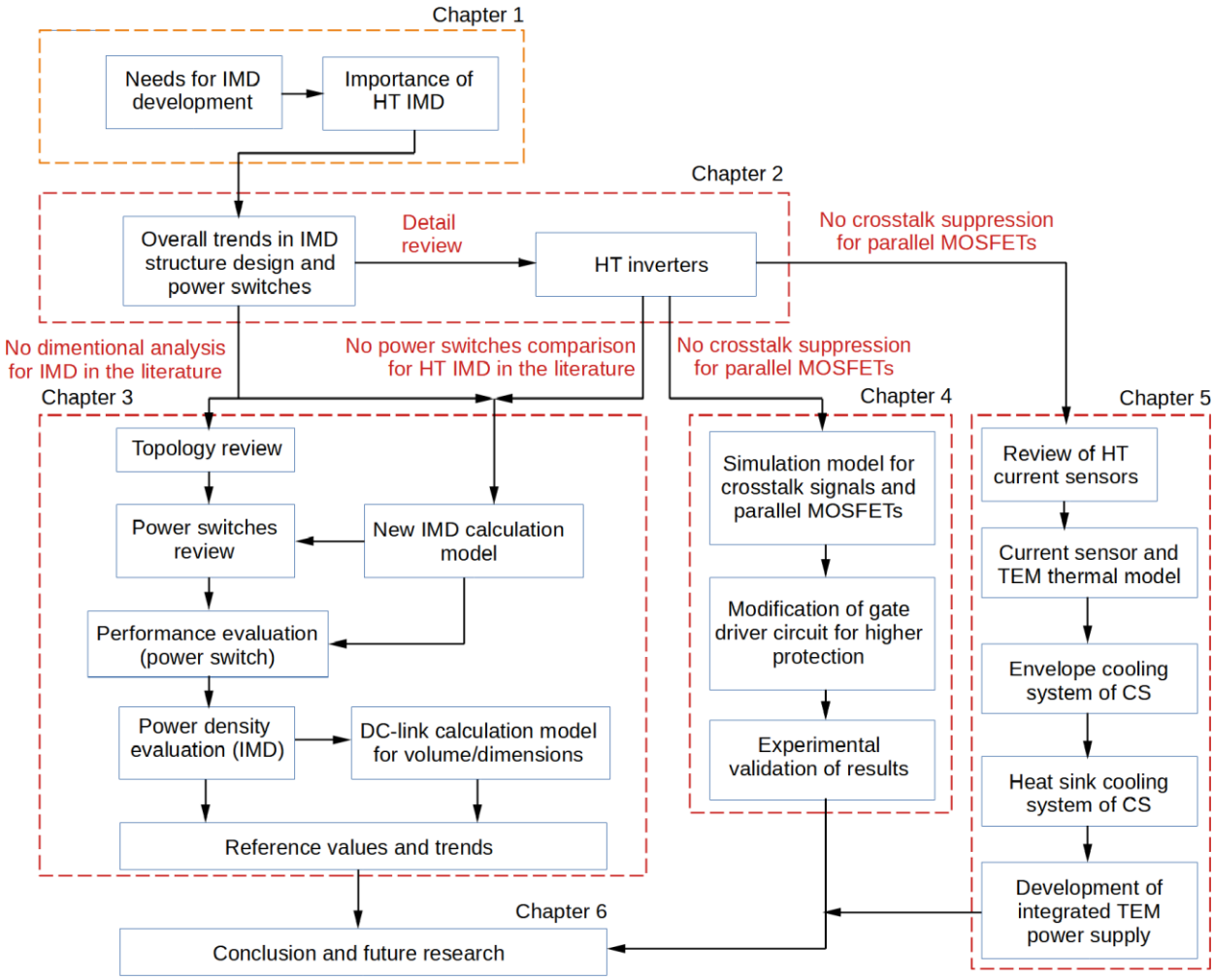


Figure 11 – Diagram with links between the thesis chapters.

Chapter 2

2 State of art in power electronics of IMD and related technologies

2.1 Integration and its recent trends in literature and industry.

The term “integration” regarding the structure of a motor drive system implies that the motor and the power inverter form a single unit that can operate without additional connections in between. Due to the long history of IMD development since the first introduction in the 1980ths[21], many variations in structure and appearance are presented both in the industry as commercial products and in literature as prototypes or concepts. Several main classifications of IMD are listed here to give a brief introduction to the topic:

Classification due to IMD modular structure (simplified structures are in Figure 12):

- *Classical IMD (by default IMD)*. The motor has a solid structure, i.e. its stator/rotor cannot be disassembled into smaller parts without damage. The inverter can operate only when fully assembled into a single package and cannot be separated mechanically into several independent equal parts. Usually, the design provides higher power density figures by comparison with other structures due to the absence of connection lines between segmented parts and repeated elements (controllers, sensors, power supply, etc.) inside the drive. All commercial drives observed in the literature review belong to this category (see Table A3).
- *Integrated semi-modular motor drive (ISMD)*. This class of IMD includes devices that have only one modular part or part that is built by combining several identical slices into a single unit. The second part of the drive has a traditional design. In most cases, ISMD does not differ functionally from classical IMD, but a different name helps highlight the distinct structure of the prototype.
- *Integrated modular motor drive (IMMD)*. It is a relatively new branch of IMD evolution (the first paper in the literature used was published in 2013 [22]). An IMMD is usually divided into several equal blocks (including the stator core and the winding). While assembled, blocks are connected in a serial or parallel system with some redundancy of switching devices; therefore, such structure, in theory,

could provide higher robustness than the classical one. Another attractive feature of the modularity is that a new block could easily replace the damaged one in case of failure. There is no reported IMMD available for commercial exploitation found during the literature review, and only laboratory prototypes with different percentages of technology implementation are mentioned in the literature ([23], [24], [22]). High-speed synchronization between modules is crucial for efficient operation.

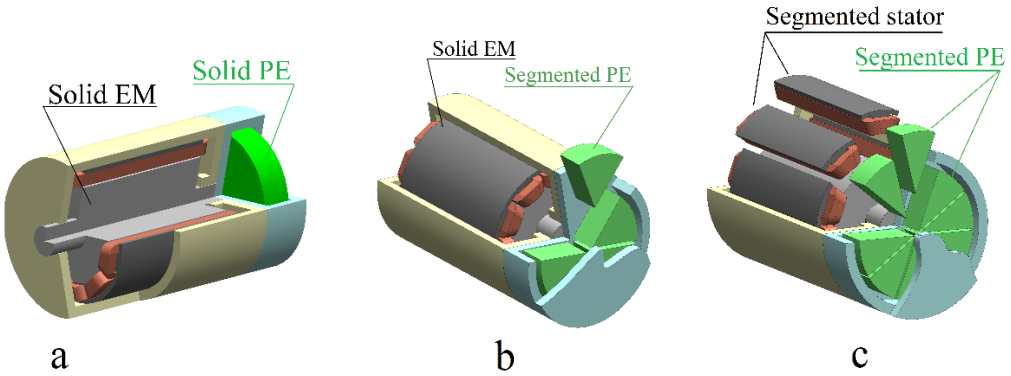


Figure 12 – IMD classification based on its structure modularity (a – IMD, b – ISMD with segmented PE, c - IMMD).

IMD could be divided into several classes according to the position and orientation of PE to the motor housing:

1) *Inner/External* (*I/E*). Inner PE (PCBs and modules) occupies space inside the machine housing, sharing the same cooling contour and thermally interacting with EM. There are quite a few examples of IMD with inner PE in the literature review for power levels of more than several kW. Thermal management and convenient access to PE components might be challenging for IMD with the inner location of PE. External PE has lower thermal interaction with EM due to separated cooled volume. Easier thermal conditions could be why IMDs with external PE locations are more widespread (see Figure 17). Figure 13 illustrates the difference between these two structures.

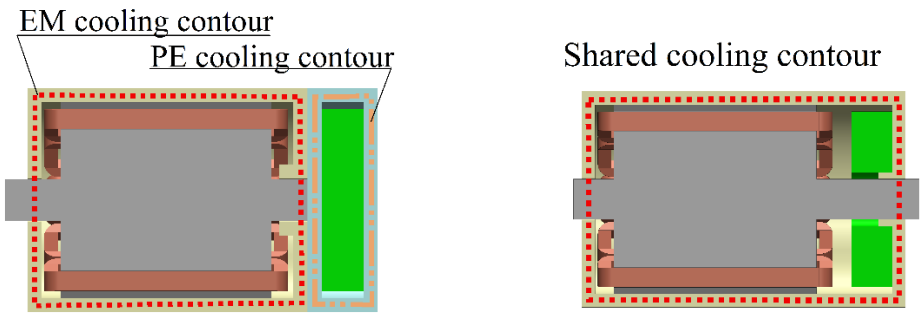


Figure 13 – Examples of external (left) and inner (right) location of PE.

2) *Axial/Radial/Circumferential/Top(A/R/C/T)* – orientation of normal vector of PE PCB or housing regarding the machine's axis of rotation (see Figure 14 for detailed explanation). Top orientation is a case of radial when PE is implemented as a single box and located only on one side of the machine. It is one of simplest and popular ways to integrate EM and PE as it offers more freedom in terms of PCB shape, volume etc than other structures.

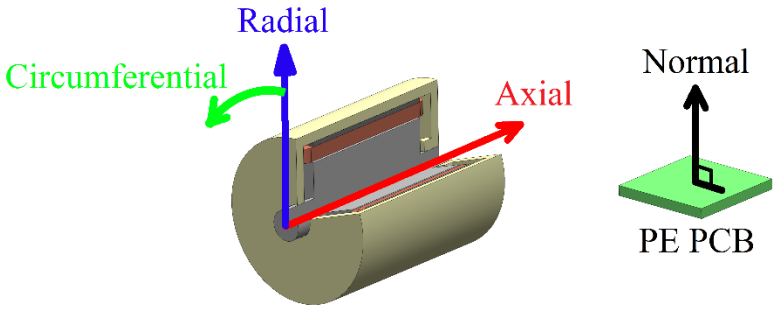


Figure 14 – Classification for different orientations of PE PCB's normal vector with respect to the machine's axis of rotation.

3) End plate/Stator (Ep/S) – characterizes the location of PE with reference to parts of machine housing (see Figure 15).

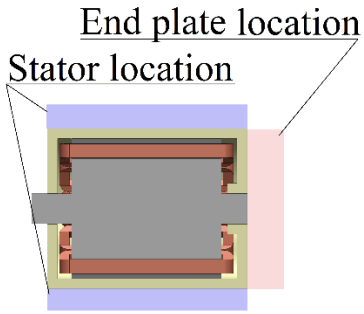


Figure 15 – Examples of end plate and stators accommodations of PE elements.

Examples of structure design for the most of options are presented in Table 1. Although the classification includes many theoretically possible designs, several options have

significantly more complex mechanical structure (for example, those with circumferential orientation) and, most probable, higher difficulties in manufacturing. A number of parameters are indicated in the table to characterize dimensions of each design. Normalized increase in IMD diameter D_{IMD}/D_{EM} show relative difference in outer diameters between the motor and whole system. Normalized increase in total length $\Delta L_{ADD}/R_{EM}$ is used when PE locates after EM. The machine does not have any particular length in the analysis, so its stator radius is used as reference parameter. PE volume $V_{PE\ CASE}$ is normalized by $V_{PE\ CASE\ EAEp}$ to demonstrate the difference in weight of housings for different designs, as it might be important for weight-restricted applications. Supplementary parameters used for calculations are described after the table.

Literature review includes over 35 samples of various IMD types from industry and academia to show a variety of implemented technologies and structures. Due to distinct and simplified thermal management (mostly natural air convection by motor housing) many commercial low power IMDs (peak power less than several kW) are not included in the list. Samples are divided into three groups based on the stage of the project's lifecycle to indicate the technological feasibility and commercial success of a certain design. Group "Concept" includes samples described only by simulation and 3D modeling without evidence of an actual prototype (not presented in the same paper or next publications). These designs usually present some new trends or ideas without (or limited) engineer postprocessing. Group "Prototype" includes IMDs with a real sample built and tested. Group " Product" consists of commercial products that could be purchased separately or as a part of another device; thus, the group presents the most mature technologies from manufacturing points of view. At the same time, this group is affected by non-technical factors such as logistics, expenses on manufacturing and design, maintenance costs, etc. Detailed information about all drivers is presented in Table A1, Table A2, Table A3 for groups "Concepts", "Prototypes", and "Products" respectively.

The overall view of IMDs is presented in Figure 16 with peak power and year when it was mentioned in literature first time. Projects with WBG semiconductors are marked to indicate the difference in the spread of new materials in academic research and industry. First reported prototypes of IMD with high power levels were developed by 2006 ([25],[26]). In 2012 two EV powertrains with IMD from Nissan and Tesla finished testing and became available for the market. Since then, scientific interest in IMD remained almost the same with a gradual increase in inverter peak power. WBG semiconductors have been almost the only material used in concept and prototype projects since 2015,

showing the fast adoption of new components by academic researchers. By 2015-2016 automotive industry accepted integration technology as a standard, and four new IMD became available. Most inverters were built with Si IGBT modules which remained the most popular semiconductor type of power switchers until recent years. A few inverters were reported as fully SiC by the end of 2021. An increased number of presented IMD and a rise in their peak power could be noticed as a general trend.

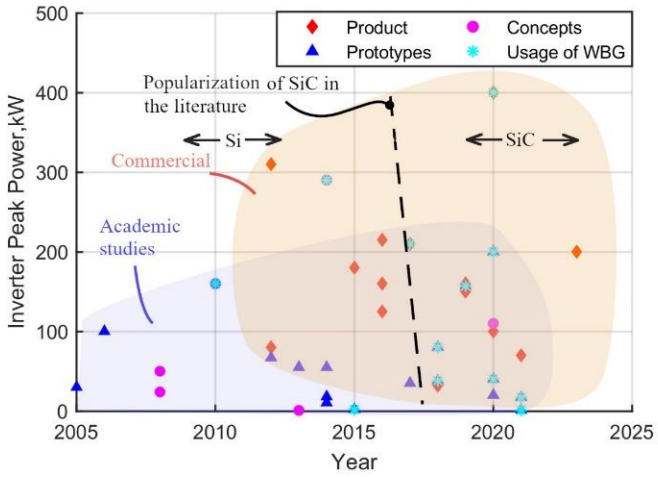


Figure 16 – Inverter peak power for industry/academic designs over 2005- 2022 and usage of WBG components.

Distributions for various drive's structures among considered IMDs are presented in Figure 17. Non-modular IMD is still the most popular structure for both research and industry is the classical IMD. Although research projects (both prototypes and concepts) are presented in all categories, there are no commercial products in modular and semi-modular types. Such difference could be explained by manufacturing and control difficulties at the current technological level.

Table 1 – Examples of structure design for different PE locations and orientations.

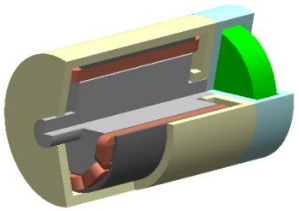
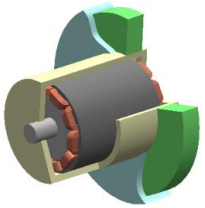
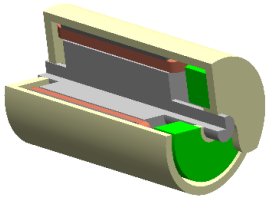
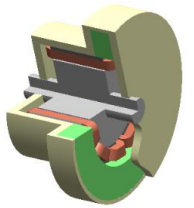
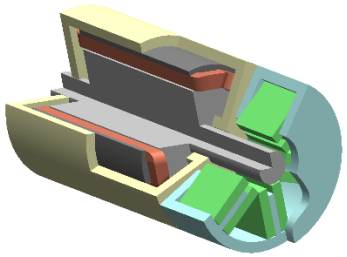
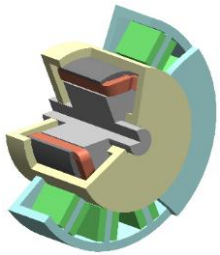
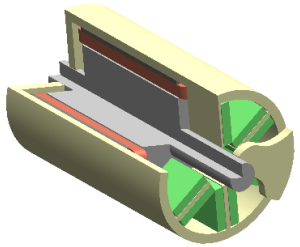
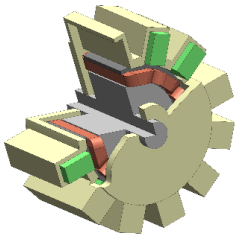
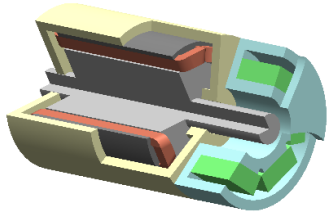
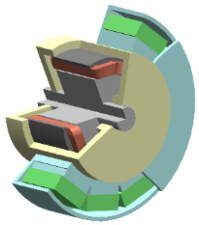
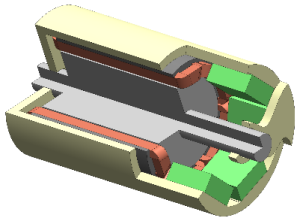
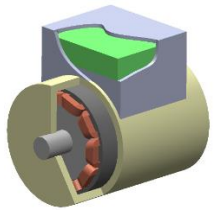
		External PE (individual cooling contour and housing for EM and PE)				Internal PE (cooling contour common for EM and PE)			
		End plate location		Stator location		End plate location		Stator location	
Axial	D_{IMD}/D_{EM}	1	EAEp	1.42	EAS	1	IAEp	1.4	IAS
	$\Delta L_{ADD}/R_{EM}$	0.33		-		0.25		-	
	$\frac{V_{PE}}{V_{PE\ EAEp}}$	1		1		0.97		1	
	$\frac{V_{\text{PE CASE}}}{V_{\text{PE CASE}\ EAEp}}$	1		1.1		0.2		0.85	
		- Single-board – for simple topologies; - -Simple inverter assembling;		-Simple inverter assembling; - external axial air cooling;		-Simple inverter assembling; - Single-board;		-Simple inverter assembling; - external axial air cooling;	
Circumferential	D_{IMD}/D_{EM}	1	ECEp	1.29	ECS	1	ICEp	1.3	ICS
	$\Delta L_{ADD}/R_{EM}$	0.67		-		0.62		-	
	$\frac{V_{PE}}{V_{PE\ EAEp}}$	1		1		1		1	
	$\frac{V_{\text{PE CASE}}}{V_{\text{PE CASE}\ EAEp}}$	1.73		1.45		0.85		1	
		- Multi-board inverter; - internal axial airflow cooling;		- Multi-board inverter; - - external axial air cooling;		- Multi-board inverter; - internal axial airflow cooling;		- Multi-board inverter; - external axial air cooling;	

Table 1 continue.

		External PE (individual cooling contour and housing for EM and PE)				Internal PE (cooling contour common for EM and PE)			
		End plate location		Stator location		End plate location		Stator location	
Radial	D_{IMD}/D_{EM}	1	EREp	1.31	ERS	1	IREp	1.12	ETS*
	$\Delta L_{ADD}/R_{EM}$	0.7		-		0.5		-	
	$\frac{V_{PE}}{V_{PE\ EAEp}}$	1.16		1.1		0.87		1	
	$\frac{V_{\text{PE CASE}}}{V_{\text{PE CASE}\ EAEp}}$	1.3		1.42		0.38		1.04	
		- Multi-board inverter; - internal axial airflow cooling; - Simple inverter assembling;		- Multi-board inverter; - external axial air cooling; - Simple inverter assembling;		- Multi-board inverter; - internal axial airflow cooling;		- Single-board – for simple topologies; - Simple inverter assembling;	

*- feasible IRS structure is a subject of mechanical and thermal analysis as significant stator surface should be occupied by PE, so ETS is presented instead.

D_{IMD} – Maximum diameter of IMD housing, D_{EM} – diameter of EM housing; ΔL_{ADD}– increase in the length of IMD due to PE part, R_{EM} - radius of EM stator, V_{PE} – volume of PE part, $V_{PE\ EAEp}$ - volume of PE part for EAEp design, $V_{\text{PE CASE}}$ – volume of PE case material, $V_{\text{PE CASE}\ EAEp}$ - volume of PE case material for EAEp design.

All designs have the equal area of PE attached to a heat sink, so all IMD can accommodate the same number of power devices. Height of PE PCB (green cuboid) $H_{PE} = 0.25R_{EM}$ and wall thickness $T_W = 0.04R_{EM}$ is also the same for all IMD, however the total PE volume V_{PE} could vary due to different shape of PE part. EAEp structure is used as a reference because of the simplest design.

The distribution of the most popular types of power switching devices throughout all IMD is presented in Figure 18. Custom-made solutions and various commercial devices form two equal groups. Although there is no dominance of custom power modules in academic research due to complex manufacturing, this kind of switchers is preferred in the industry (for the observed set of commercial drives). In most cases, a power module consists of a half-bridge structure capable of handling the full range of motor phase current; therefore, paralleling of power switches is almost not found in commercial products. The only well-known examples of commercial products with wide usage of parallel devices are Tesla's traction inverters. At the same time, the growing process of SiC crystals is more challenging than Si[27]. This might give an advantage for applications with smaller SiC devices as suppliers can deliver them to customers earlier in the required quantity. In turn, electrical engineers finish the development faster, and then serial production can also start earlier.

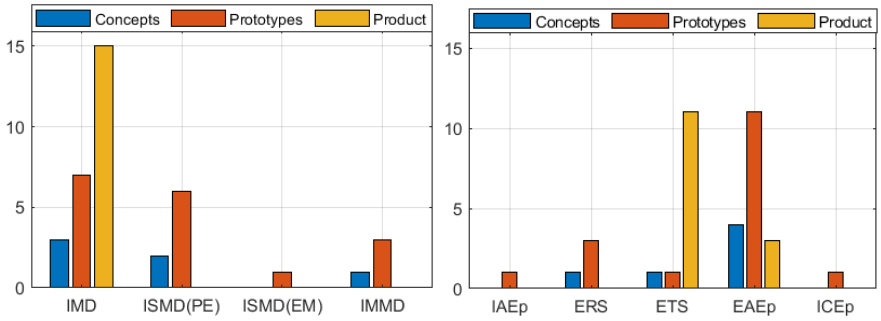


Figure 17 – Distribution of IMD structures

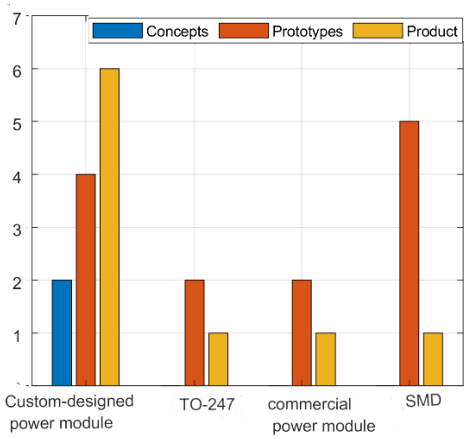


Figure 18 – Distribution of switching devices in IMD reviewed.

The example of Tesla model 3 proved the noticeable advantages of SiC over typical Si. Gravimetric power density of Tesla model 3 fully SiC inverter is 43kW/kg which is the highest among other drives with known figures presented in the review (see Table A3 for details). Likely, other companies will present their own fully WBG inverters soon.

Considering the aforementioned data, the following trends have been noticed and are reported in Table 2

Table 2 - Recent trends in commercial IMD

Trend	Description
OEM traction drive for automotive industry	Manufacturers provide more electric drive units (EDU) as a single module with an integrated motor, an integrated inverter, and a gearbox [28-32]
IMD structure	*Drive modularity* Some manufacturers offer IMD design that allows to combine two EDUs and form a parallel connection to scale total output mechanical power[33]. *Adoption of new form-factors in commercial IMD products* Different structures (not only ETS) became more popular in automotive industry[29, 34].
Inverter	*Wider usage of SiC devices in traction inverters*

2.2 Design procedures and algorithms.

Standardized design procedures, as a set of rules and stated relations between parameters, could be a valuable instrument for IMD evaluation or optimization when the initial characteristics of devices and the system vary in a wide range and affect the overall performance (or other target parameters) in some complex way. IMD design procedure should include both calculation models (or a dataset with calculation results) of the motor and the power electronics to account for their electrical and mechanical interconnections and obtain accurate results. In the case of ETS configuration, two parts have limited mutual influence from thermal and mechanical points of view; therefore, usually, they could be analysed separately. By contrast, EAEp configuration might require more significant mutual influence of these two parts, and motor structure should be considered during the inverter's development.

Recently some publications presented a structural approach to various converter designs to highlight relationships between different parameters and characteristics of the device. Summary of reviewed methods with pros and cons is described in Table 3. For example, in [35], the AC/AC converter analysis focuses on relationships between efficiency, output current, topology, and chip area. The proposed algorithm calculates the minimum chip area with account for the motor type and power, characteristics of semiconductors etc. At the same time, it does not use any real prototypes of power switches, and the model of the cooling system is simplified to a single value of area thermal resistance. Calculation of switching losses does not include compensation for gate resistance and temperature. In design procedure flowchart explains. In [36], parametric analysis determines the

relationships between efficiency, volume, and power density. Higher losses at higher switching frequency cause an increase in heat sink volume, a decrease in overall power density, and a decrease in transformer dimensions. The diagram presents the trade-off, and the Pareto front is highlighted. The method of indicating the correlation between electrical parameters (efficiency, temperature etc.) and dimensions (weight, volume etc.) could be applied to IMD. The paper does not include different types of switches and cooling, so more advanced techniques should be developed to calculate power losses and thermal conditions of power switches. In [37], optimization analysis considers motor and inverter characteristics to determine optimal values of some design parameters. The correlation between total drive weight and power losses is well presented with different initial conditions. Power electronics is built with only one type of switches without paralleling; therefore, the physical characteristics of switches are constant throughout the research. The cooling system includes an air-cooled heatsink with constant case-ambient thermal resistance that scales with changes in power losses. This study shows deep electrical relationships between these parts, but no mechanical limitations for the inverter are imposed by the motor structure.

Table 3 – Studies with highlighted design algorithms

Device Type	Analysis	Limitations	Year	Ref
VBBSC	Torque, Efficiency/Topology, Chip area	No Rds on(Tj), no real devices, no volume analysis	2009	[35]
Dual active bridge	Efficiency, Volume/Power Density, switching frequency	One type of MOSFET, one type of cooling	2019	[36]
Motor drive (Motor+VBBSC)	Weight/losses optimisation with 14 input parameters	Not detailed analysis of PE part; Mechanical influence of integration is out of analysis;	2020	[37]

Although the separate design algorithms for motors and power electronics are widely presented in the literature, the united scheme is rarely explained. Therefore, the generalized design procedure with a large variety of input parameters is an actual research topic for optimization and demonstrative purposes.

2.3 Cooling technology in power electronics of IMD.

Thermal management of IMD inverter is a complex multi-disciplinary system of several semi-independent components (a power switch, PCB or baseplate, a cold plate, etc). The main aim of a cooling system is to remove a significant amount of generated heat and provide acceptable operating thermal conditions for power switches without deterioration

of electrical characteristics. Gate drivers and control devices usually do not require additional cooling except natural airflow convection due to relatively limited power dissipation. However, operation under HT conditions might demand extra measures to keep the temperature of control boards in the permissible range.

The cooling structure depends on the switch device type as it might have a unique design (a base plate or an integrated cooling heat sink, for instance). In general, two different groups could be distinguished that include most of the cases:

Discrete switching device with surface mount package (SMT). These devices use a thermal pad to remove heat from the die, and typical junction-case thermal resistance is about $0.4^{K}/_{W}$ (ranges from 0.16 to 1.1). SMT switches (for example, TO-263 packages) have an electric connection between the drain and the thermal pad, so the PCB has to perform both good electrical and thermal conductions and interact with a cold plate or other types of cooling. In that case, a power PCB is also included in the structure of the cooling system.

In literature, the usage of discrete power transistors in IMD is not so widely presented (see Figure 18) compared to power modules. Moreover, half of the studies do not focus on high power density and use natural air convection as the main heat transfer mechanism. In one case [38], designers use liquid cooling with typical FR-4 material enhanced by thermal vias to obtain moderate thermal resistance of PCB without manufacturing difficulties. A drawback of this approach is the significant thermal resistance of insulating material/thermal interface material that prevents electrical contact between PCB traces/thermal vias and the heatsink surface. The reported value of PCB to ambient thermal resistance reaches 12 $^{K}/_{W}$, which is not acceptable for MOSFETs with high power losses. Moreover, the mechanical characteristics of FR-4 PCB make it challenging to maintain the minimal and constant thickness of the insulation layer over large areas. Therefore local hotspots and non-equal heating are possible[39].

Advanced PCB materials could be used to increase heat transfer coefficient of PCB, for example, insulated metal substrate (IMS). Typical thermal resistance lays within 0.5-1 K/W per cm^2 which is lower than for FR4 PCB with thermal vias.

Commonly used thermal stacks for SMD switchers are shown in Figure 19.

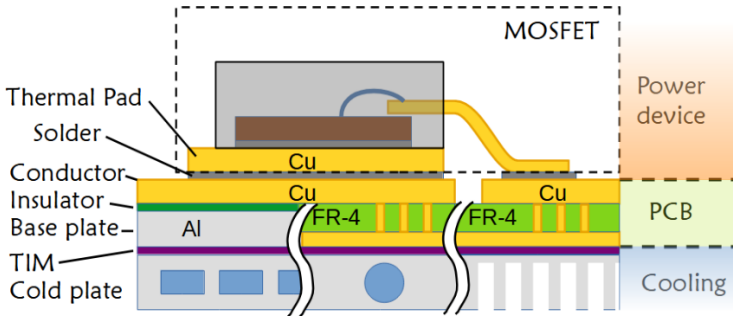


Figure 19 – Reported cooling stack for IMD with discrete components
(IMS with water cooling[29], FR-4 with liquid cooling[38], FR-4 with air cooling[40])

Although they are rarely presented in the IMD literature together with discrete components, ceramic PCB is a well-known technology in high-power electronics due to its high insulation characteristics and thermal conductivity (typical is 25 $^{W}/_{mK}$ for Al_2O_3, the maximum is 180 $^{W}/_{mK}$ for AlN). The ceramic substrate is widely used in power module fabrication as a heat interface layer and an insulator. In some cases, it might be reasonable to use ceramic substrate in combination with high-performance cooling to obtain an effective way for heat dissipation. In [41] and [42], two different versions of custom-made power modules are presented with ceramic PCB made by Direct Copper Bonding (DBC) technology. Authors use SiC dies, however, the same approach is suitable for SMT power components. Advanced jet direct cooling applied in the project should provide high overall thermal conductivity, but no figures for experimental or simulation thermal resistance are released. Design of the single switching module with cooling system is presented in Figure 20.

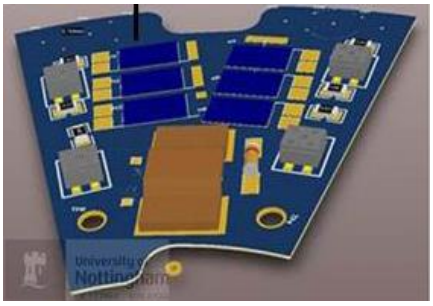


Figure 20 – Example of ceramic PCB for power electronics of IMD [42].

Another advantage of ceramic board is the absence of poor heat conductive insulation layer that becomes a “bottle-neck” for IMS solutions (see Figure 21). SMT MOSFET packages feature a small area (about 50 mm^2) of thermal pad. Unfortunately, in IMS PCB only a thin (usually 70-200μm) copper layer performs initial heat spreading along the surface of PCB. If PCB insulation layer (called prepreg) has low thermal conductivity, its impact on total thermal resistance might be significant. Then an increase of transferring

heat area is essential for its reduction. Although specific thermal resistance of both IMS and ceramic PCB through the board $\Theta_{S\,TH}(\frac{m^2K}{W})$ have comparable values, ceramic PCB has noticeably higher thermal conductivity along the PCB surface $\Theta_{S\,PAR}$, so larger area participates in heat transfer.

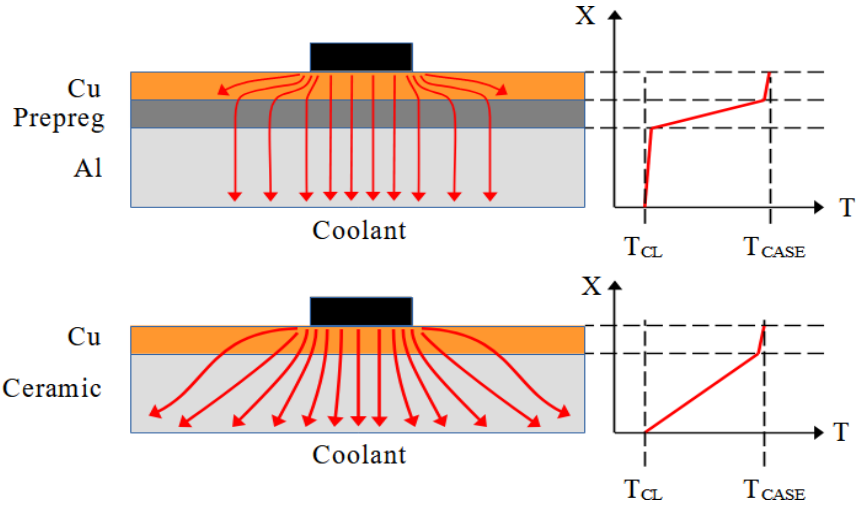


Figure 21 – Heat spreading and temperature distribution in IMS and ceramic PCBs with typical value of Θ_{HS-A} for water cooled cold plates (Θ_{HS-A} is comparable with $\Theta_{Ceramic}$).

The influence of PCB thermal resistances on total junction-heat sink thermal resistance is demonstrated in Figure 22 (thermal resistances of MOSFET and TIM are typical values). It is noticeable that the impact of PCB becomes limited for high-grade ceramic materials.

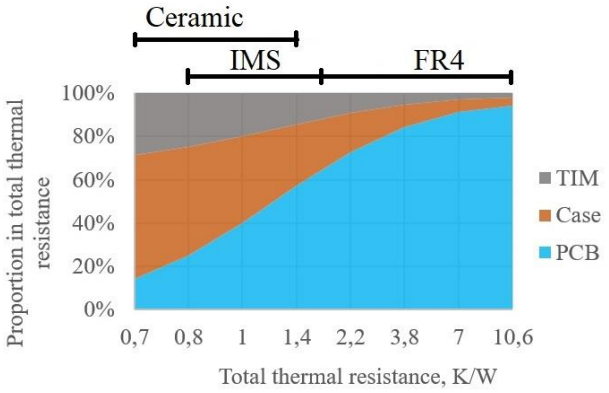


Figure 22 – Total thermal resistance for SMT MOSFET with different PCB material ($\Theta_{J-C} = 0.4\ ^{K}/_{W}$, $\Theta_{TIM} = 0.5\ ^{K}/_{W}$, $S_{PCB\ AREA} = 1.5\ cm^2$)

Discrete switching device made by through-hole technology (THT). Another type of discrete MOSFETs has a THT package (for example, TO-247) which usually does not use a thermal pad as an electric conductor. Thus, PCB could be excluded from the thermal stack, giving more freedom in selecting insulation materials and heat sink structure. Usually, the package offers larger thermal pad's area than SMT versions and higher heat

transfer capabilities. Typical junction-case thermal resistance is about $0.4^{K}/_{W}$ (ranges from 0.16 to 1.1), and resistance of insulation layer has average value of $1\ ^{K}/_{W}$ (mica+grease).

Power modules with base plate (with or without surface modification).

Several advanced methods of heat transfer have become available for power modules thanks to their complex inner structure and developed package. For example, in contrast with discrete transistors, modules can be cooled at both sides of their cases (double side cooling, DSC) with an increase in thermal performance by up to 30%[43]. Nowadays, DSC technology for discrete components is still under development, with only a short list of components available either with top or bottom (not with both at the same time) locations of the thermal pad. It is worth mentioning that most DSC modules are custom designed for the use of automotive companies, and they are not presented freely on the market.

Due to embedded insulation inside a power module, its base plate can be connected to a cooling surface without an additional insulation layer. If the coolant does not have contact with the power device (i.e., sealed inside a cold plate), the cooling is called indirect a cold plate (indirect cooling, Figure 23 b, d) or can be cooled by direct contact with the coolant itself (direct cooling Figure 23 a, c). In turn, the direct variant provides another 30% of the increase in cooling performance due to the elimination of TIM and additional metal layers [44]. Typical cooling technologies applicable for power modules are demonstrated in Figure 23.

Modules with direct cooling might have some surface modification of their baseplate to form even water-flow pattern (pin array, wave fins, etc)[26]. Also, pins create an extra area of heat exchange and, therefore, decrease the total thermal resistance of the power module. Theoretically, the method could be used with discrete components and advanced types of PCB, although it is not yet presented for IMD in the literature.

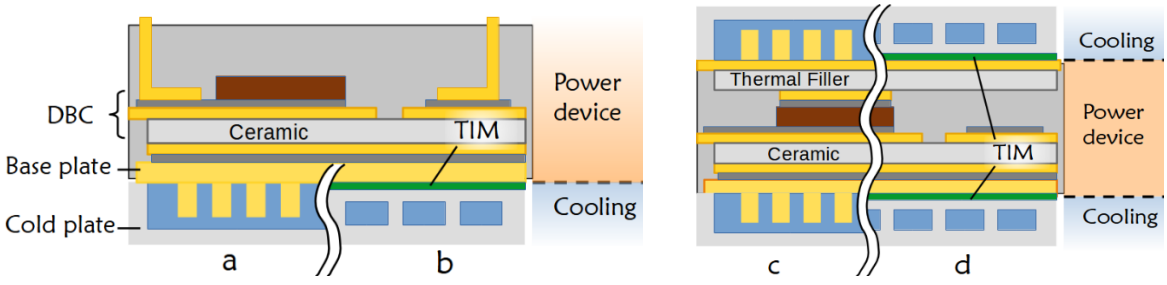


Figure 23 – Typical cooling technologies for power modules
(a, b – single side cooling; c, d– double side cooling; a, c – pin fin direct cooling; b, d – indirect cooling)

There is a special type of power modules that has an integrated cold plate instead of typical solid heat-spreading baseplate (details could be found in [45], simplified structure

is presented in Figure 24). In this case, an engineer does not need to design a cooling structure, but only provide required characteristics of the coolant.

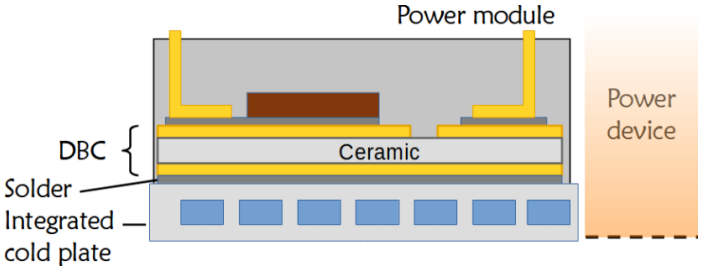


Figure 24 - Typical cooling stack for power modules with integrated cold plate.

Wider usage of power modules in IMDs also affected the diversity of cooling types used with discrete components. According to the IMD review (see Table 4) only two inverters with discrete elements out of 6 use materials with high thermal conductivity to cool power switches. These papers do not show parametric analysis of IMD thermal management and do not study deeply the influence of cooling system on PE performance and power density. Correct estimation of cold plate's thermal resistance is important to maintain manufacturing complexity of the design in reasonable range.

Table 4 – Summary of thermal stacks used in IMD

Type of devices	Cooling technology	Quantity	Reference
Discrete switches	FR-4, Air	2	[43],[40]
	FR-4, Indirect, liquid	2	[46], [47]
	IMS, Indirect, Liquid	1	[29]
	TO-247, Indirect, Liquid	1	[48]
Power module	Indirect, 1 side	4	[49], [50], [24], [51]
	Direct, 1 side	5	[26],[52], [53], [54], [42]
	Indirect, 2 sides	2	[55], [56]
	Direct, 2 sides	2	[57], [58]
	Integrated, 1 side	1	[14],[45]

Review of cold plate types and methods of direct cooling

Nowadays, designers have many options to build a cold plate with required characteristics for any kind of power devices.

Pipes/Channels. The coolant channel is formed by a metal pipe or a milled groove in the metal plate. This type features the simplest design, low manufacturing difficulty, and high robustness due to the large section of the channel (no clogging). On the other hand, the design is sensitive to layout of the channel, so hotspots are possible if the coolant channel covers the surface with blank areas. The average heat transfer coefficient is from 0.17 to

0.33 $^{W}/_{cm^2K}$ (at 1 GPM, [59]), and the cooling performance highly depends on the coolant flowrate.

Channels with fin structure. Fins placed along the flow path of coolant increase heat exchange area and make uniform flow patter over large area. In addition, the flow has higher level of turbulence, and the fin cold plate removes heat with higher efficiency. The design and manufacturing processes demand more efforts than the simple channel structure. Shape, size, and location of the fins influence heat transfer coefficient. Moreover, flow pattern should be analysed carefully to avoid uneven coolant distribution and zones with low coolant velocity. The average heat transfer coefficient is from 0.25 to 1 $^{W}/_{cm^2K}$ (at 1 GPM [59, 60]). Wave fins are a combination between fin structure and single channel cold plate design, as wave fins create several separate (or partially separate) liquid paths in the direction of the coolant flow. It helps to reduce the temperature gradient and increase heat exchange area.

Microchannels. The cold plate consists of a large number of microchannels (the height is less than 1mm) connected in parallel providing efficient coolant distribution and high heat exchange rate. At the same time, coolant temperature has a significant gradient along the flow direction, therefore it is challenging to use microchannels for large cold plates. Another drawback is that narrow passes of microchannel cooling are sensitive to the quality of the coolant and require filtering to keep the system in operating conditions. The average heat transfer coefficient is 2.4 $^{W}/_{cm^2K}$ ([61]).

Jet impingements. The coolant jet is directed towards the heat source and fired under high pressure to create an intensive heat exchange process at the designated area. Jets can form a regular array to cool relatively large area with evenly distributed heat transfer. At the same time, a single jet (or a small group of them) can be used to cool a particular element with direct cooling. The design process of jet cold plate requires to perform multi-physics calculations for nozzle geometry optimization. The performance of complex array structure is also sensitive to pressure distribution, and incorrect layout of nozzles might affect outgoing coolant velocity and create a local overheating. Additional space is required to accommodate nozzles, an inlet and an outlet distribution channels, increasing the height of the cold plate. The average heat transfer coefficient is 2.4 $^{W}/_{cm^2K}$ (range 0.17-14.2, [62]).

Spray cooling. The cold plate is similar to a jet cold plate, with coolant going out through nozzles under high pressure. In contrast with jet cooling, small drops created by the nozzle are used to remove heat from the heat sink surface. These drops create a thin

coolant layer covering the surface of the heat sink and efficiently removing excessive energy from it. Spray cooling also requires space for nozzle accommodation and spray chamber, so the overall dimensions are larger than typical cold plate. The average heat transfer coefficient is 1.6 $^{W}/_{cm^2K}$ for the single phase cooling (ranges from 0.9 to 7.1, [63]).

The last three methods also can operate in 2-phase mode when the coolant evaporates from the hot surface if its temperature reaches a specific threshold value. The efficiency of 2-phase cooling is significantly higher than that of 1-phase methods [64], but the complexity of the cooling system also increases as designers have to deal with a mix of liquid and vapour coolant at the output of the cold plate.

The summary of cooling technologies commonly used in power electronics is illustrated in Figure 25.

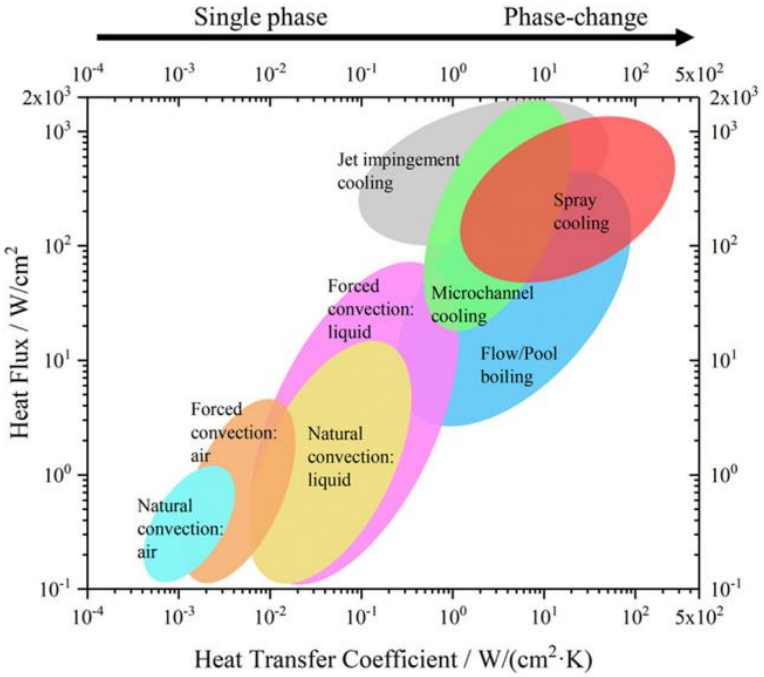


Figure 25 – Comparison of different heat transfer methods [65]

There are several important characteristics of thermal management and the IMD itself that play significant role in selection of proper cooling method:

1) **Target heat exchange coefficient of a coldplate (h_{CP}).** Thermal capabilities of cooling system should be comparable with heat transfer capabilities of power device's thermal stack. Very high h_{CP} does not improve total thermal resistance θ_{J-Amb} of assemblance if other layers have poor thermal conductivity but might increase development and manufacturing cost (see Figure 26).
2) **Complexity of design process, manufacturing, and operating conditions** should

be evaluated, as coolers with high h_{CP} (especially types with two-phase cooling) require understanding of heat transfer physics (bubbles creation, wetting etc.). For example, performance of jet cooling is sensitive to jets layout due to its influence on coolant pressure distribution[66]. Filtering of coolant can be an issue if the cooling involves tiny channels or holes.

3) **Maximum coolant pressure.** This parameter could be important in case of direct cooling due to limited capabilities of seal materials and the baseplate itself. Typical values of maximum pressure for O-rings do not exceed 15bar without special measures (better materials or higher tolerance of manufacturing), and relative maximum pressure for commercial power modules with a metal baseplate is only 2.5bar. It is strictly forbidden to violate these restrictions due to possible damage to the module (deformation) and coolant leakage. Indirect cooling usually is not affected by the issue thank to its robustness and thickness of metal.

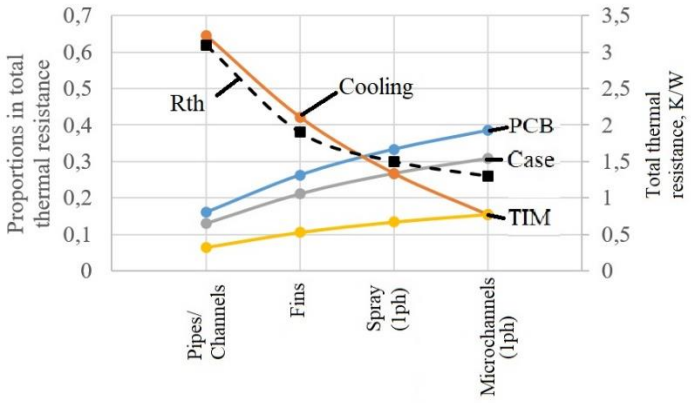


Figure 26 – Influence of cooling method on total thermal resistance for SMT MOSFET with IMS (heat transfer coefficients are typical for 1GPM coolant flowrate)

Among the reviewed IMDs, preferable choices are cold plates with simple water channels and pin fin structures (see Table 5). Cold plates with water channels are easy to design, and they do not require advanced manufacturing to produce. Pin fin cold plates usually are the most effective commercially available heatsinks, however, the only rectangular shape with standard dimensions is available.

Table 5 – Variety of cooling techniques in IMD prototypes

Cooling technology		Number of prototypes	References
Pipes/Channel		4	[48], [24], [46], [49]
Fins	Wave	2	[53], [55]
	Pin	6	[26], [51], [52], [54], [57], [58]
Microchannel/flat channels		2	[14], [56]
Jet		1	[42]

2.4 High temperature power electronics in IMD.

High-temperature power electronics for power converters is still a subject for research due to the thermal limitations of packages[67]. Moreover, analysis of recent publications in HT power electronics shows that thermal issues of packages prevent further research progress in this area.

Well-known electronics made by silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) were the only choice for engineers and researchers till recent years if extreme operating conditions were required. Such components are expensive, limited in performance, and generally unavailable for civic applications. Therefore, the area of HT power electronics applications traditionally belongs to very specific industrial, military or space fields with strong government support. Due to security clearances and trade secrets, the related information is usually outdated or not available. This situation did not change until the popularization of EV/HEV happened in the early 2000th. Electrification of private transport raised new challenges for power electronics in thermal management and mechanical structure. The idea of a unified cooling system and housing integration with combustion engines became popular. The average temperature of engine cooling is more than 105-115 C ([18]), so ordinary commercial Si power devices experience excessive heat load and reliability issues. However, the standard HT components are too expensive and cannot satisfy price requirements and production rates. Enhancement of classical Si materials and overall technological progress resulted in serious improvement of power modules' characteristics (lower ohmic resistance, better thermal conduction, reduction in parasitic inductances, etc.). As a result, several HT prototypes were designed and built with Si IGBT power modules. In [49], the authors use a commercial IGBT Si HB power module (650V, 150A), indirect cooling with an ordinary multichannel round cold plate. Thermal FEA simulation shows that difference between coolant temperature and junction temperature of IGBT does not exceed 15K, thus the design is capable of maintaining a safe margin for T_j at $T_{CLNT} = 115℃$ and relatively low maximum output power. In [26] custom Si IGBT power module (600V, 320Arms) utilizes direct cooling with a diamond-shaped fin structure over the whole chips' area achieving junction-coolant heat transfer coefficient $h_{j-c} = 2.2\ \frac{W}{Kcm^2}$. It is mentioned that the junction temperature rise does not exceed 40K, and the inverter can operate at coolant temperature of 115℃.

A noticeable example of HT power electronic for EV is presented in 2007 by RINI technologies [68]. Although IGBT technology was used in this inverter, the maximum output power is 250kW with 100℃ of maximum coolant temperature. Such high values for IGBT modules were achieved by paralleling power switchers (6 IGBTs and 3 diodes per phase), elimination of a baseplate, and a two-phase spray cooling system (spray targets are recognizable on the cooler's side of the module in Figure 27). The design of power electronics is based on the power inverter SKAI 4001GD06 from SEMICRON, which is initially equipped with an integrated cold plate (its characteristics are close to pin fin technology). The new spray cooler drastically increased heat transfer performance from the typical $0.66\frac{W}{Kcm^2}$ for pin fin type to $28\frac{W}{Kcm^2}$. Cooling system is described in details in [69]. Unfortunately, there is no description for the rest part of the cooling system (pump, condenser etc.), so it is not easy to estimate its volume and other technical characteristics.

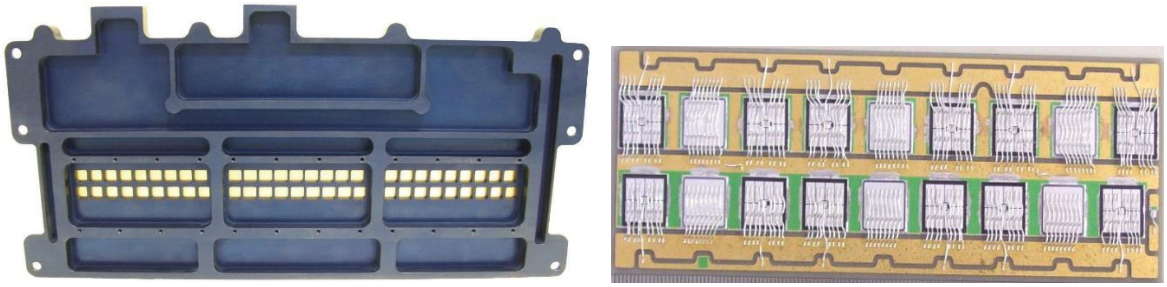


Figure 27 – Bottom side of RINI inverter with windows for direct spray cooling (golden colour) [68] and one of its inner DBC boards with array of parallel devices, top view[69].

With serial production of WBG components, researchers got an opportunity to extend power density limits, dimensions, and maximum operating temperature. In 2013 two tested prototypes of HT power converter with custom SiC modules were presented in [70] an [71]. Both devices utilize air cooling thanks to high maximum junction temperature $T_{j\,MAX}$, and junction temperature measured experimentally exceeds 220℃ for both of them. At the same time the prototype described in [70] only is able to operate at high ambient temperature (150℃), because all control chips are manufactured with SOI technology. In [19] authors also want to benefit from high $T_{j\,MAX}$ in order to operate at high ambient temperature with air cooled heatsink. According to simulation results the heatsink maximum temperature reaches 235 if inverter's output power is limited by 10kW. Thermoelectric cooling and thermal insulation protect gate drivers and controller from excessive temperature. Although the proposed cooling approach might give advantages with higher junction temperature of power modules (at least 250℃), commercial transistors presented on the market today cannot work under such conditions.

Further development of HT power devices results in a number of prototypes ([72], [73], [74], [75], [76], [77], [78]) with outstanding power density and ability to work with HT coolant (up to 115℃, detailed characteristics of inverters in Table A4). All these projects include commercial HB SiC modules (CAS325M12HM2 for high power density and CAS300M17BM2) manufactured by Cree company due to the best combination of electrical and thermal characteristics with a significant reduction in module's height (see Table 6). In Figure 28 section of CAS325M12HM2 is presented to indicate some features of its design, for example, large number of parallel devices and very wide traces for power lines.

Table 6 – Characteristics of Cree power modules

Parameter	CAS325M12HM2	CAS300M12BM2	CAB450M12XM3
Drain-Source Voltage, V	1200	1200	1200
Continuous Drain Current, A	444 (25℃)	404 (25℃)	450 (25℃) 409 (90℃)
Junction Temperature, ℃	175	150	175
Power dissipation	1500	1660	
Thermal resistance, $^{K}/_{W}$	0.1	0.07	0.11
Dimensions, mm	65*110*10	62*106*30	80*53*19
Weight, g	140	300	175

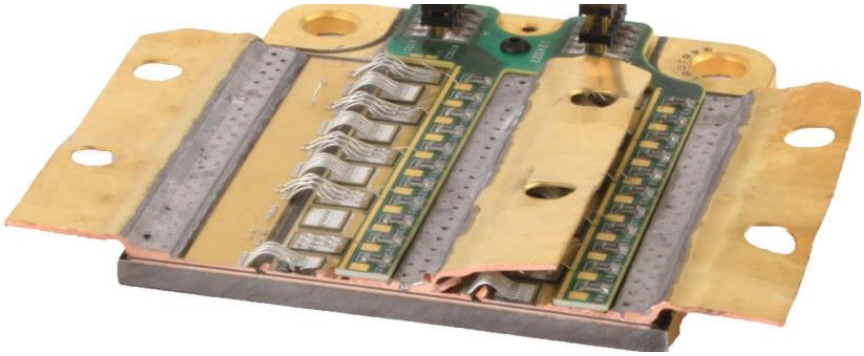


Figure 28 – Section of power module CAS325M12HM2

Most converters use cold plates with inner fins for indirect cooling as it provides enough heat transfer to keep case and junction temperatures low despite the high temperature of the coolant. This approach is quite effective if the desired parameters are high power density and maximum possible output power. Wolfspeed designed an evaluation kit to demonstrate the capabilities of its high-performance power modules (see Figure 29).

Figure 29 – OEM 300kW inverter CRD300DA12E-XM3 by WolfSpeed[79].

2.5 Conclusion

IMD is a well-known research topic and a rapidly developing field of engineering or industrial interest. It is shown above that power modules are the preferable choice for any type of IMD (especially for industrial samples), and they mostly dominate the area of HT prototypes. Module biased position of developers in terms of PE design is understandable. Advantages of power modules (such as high current, simple thermal interface, simple electrical connection, etc.) simplify the system design process. Therefore, engineers need to solve fewer serious technical problems related to the design of a power board and focus on other parts of the device.

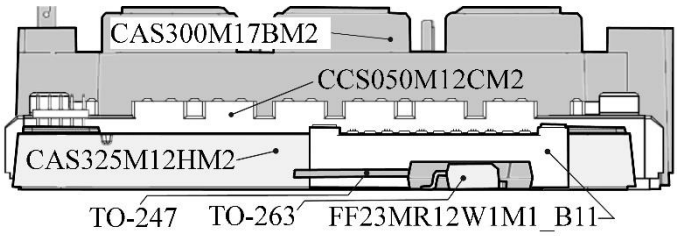


Figure 30 – Different packages of semiconductor power switches

However, there might still be applications where some characteristics of power modules do not satisfy the required conditions, and developers have to search for alternative solutions. *First*, usage of specific power components comes at the cost of reduced flexibility in terms of the geometry and shape of a converter. Pre-configured packages of power modules cannot always fit the designated area's shape and ultimately limit the optimal usage of effective space in some cases. The square or rectangular shape of power modules fits well if the inverter's case has a square shape without openings, or shape is not a crucial parameter and could be adjusted according to the module's shape. The round shape of the base might cause some extra space to be left without usage. For some applications, a specific value for the height of the inverter is required, and only the most advanced power modules can compete with discrete components (see Figure 30). *Second*, power modules are unique products produced by a few companies (only one for HT

samples in Table A4). Therefore, the components' availability and guaranteed market access become crucial for prototyping and serial production. The absence of exact components might lead to a delay in the production or a redesign of the inverter due to differences in packages.

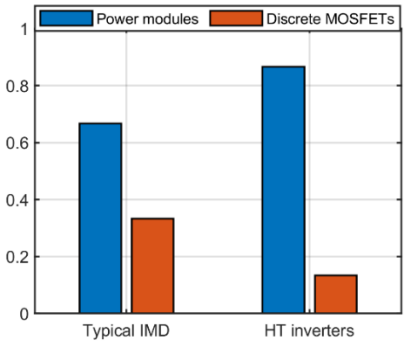


Figure 31 – Usage of different power devices in typical IMD and HT inverters.

At the same time, the capabilities of discrete MOSFETs connected in parallel to perform in such conditions are barely studied in the literature (see Figure 31). Usage of these components could be challenging in thermal management and assembling processes. On the other hand, it might be beneficial to have an alternative way to achieve comparable power levels without unique and expensive components. Parallel connection of switching devices is one of the methods in power electronics to achieve high output current, and it is successfully applied in the design of power modules (see Figure 27 and Figure 28). It is worth investigating the theoretical boundaries of discrete components in combination with different types of PCB and cooling techniques in HT applications.

Chapter 3

3 Performance analysis of PE for optimized switch selection and integration-oriented gravimetric/volumetric theoretical model of IMD

3.1 Inverter Topology

In contrast with a typical motor drive, the topology selection for IMD considers the higher number of factors related to the mechanical design of the machine and the housing. Volume restrictions and the tight layout of mechanical and electrical components inside the inverter force engineers to select fewer complex solutions in terms of switching device numbers and interconnections between parts of inverters. Moreover, system requirements, e.g., overall dimensions, location of power inputs, machine's characteristics or quantity, etc., might predetermine the structure of the inverter.

A) 3-phase 2-level voltage source topologies.

The most popular topology of the IMD inverter is the 2-level 3-phase Voltage Source Inverter (VSI) and its variations with multiplied quantity of phases due to the simplest structure and the minimal number of switching components. Simplified structure is presented in Figure 32.

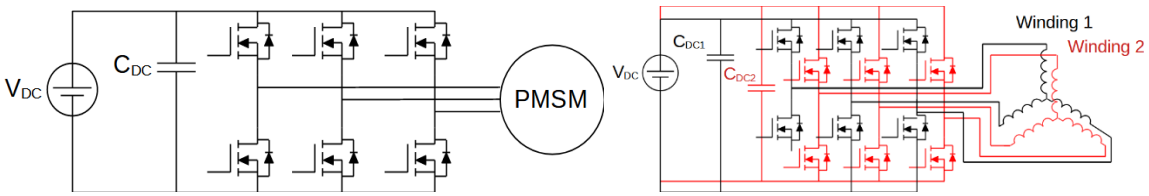


Figure 32 – 3-phase 2-level VSI (single drive – left, double channels - right).

This topology is widespread among experimental samples and commercial drivers. Many power modules, both Si and SiC in "half-bridge" configuration, are available on the market or designed by researchers. Although this topology shows approximately twice as higher total losses as the 3-level Neutral-Point Clamped topology (according to [80]), a twice lower number of switches makes the system more compact. All phases share DC-link capacitance; thus, it implies the close location of all half-bridges to reduce the influence of parasitic inductance. Therefore such topology better fits ETS or EAEp IMD structures which have only one power board. A single full-bridge structure is not a fault-tolerant

topology, and any fault of switch or phase conductor leads to inverter's malfunction. It is possible to increase its robustness either by adding extra half-bridges circuits [81] or by organizing fully parallel operations with two or more individual 3 phase structures and the same multi-winding machine (see Figure 32, [49]). Parallel connection of VSI could reduce the switching current of the MOSFET group by increasing the number of power PCBs (or 3-phase power modules) while maintaining the group area. Therefore, power connections between switching groups could be shorter, and parasitic inductance does not affect the inverter as it could in the case of large groups and long power traces. Separating the 3-phase inverter into individual half-bridge PCB is possible but requires accurate simulation of current distribution and DC voltage ripples on each module[40].

A number of studies investigate the serial connection of 3-phase 2-level inverters [43, 47] in order to use low voltage MOSFETs with a higher maximum current. Its structure is presented in Figure 33.

Total power losses for single 3-phase inverter P_{Single} and N number of series inverters P_N could be expressed as following:

$$P_{Single} = P_{cond\,S} + P_{sw\,S}, P_N = N(P_{cond\,Ns} + P_{sw\,Ns}), \quad (1)$$

where $P_{cond\,Ns}$, $P_{sw\,Ns}$ – power losses of a series inverter. If MOSFETs in both inverters are from the same type family and differ by maximum drain voltage, approximation of their characteristics could be made:

$$P_{cond\,Ns} = P_{cond\,S}\frac{R_{DS\,Ns}}{R_{DS\,S}} = P_{cond\,S}\frac{1}{B}, \qquad P_{sw\,Ns} = P_{sw\,S}\left(\frac{V_{Ns}}{V_S}\right)^A = P_{sw\,S}\left(\frac{1}{N}\right)^A \quad (2)$$

$$\frac{P_{cond\,N}}{P_{cond\,S}} = \frac{N(P_{cond\,Ns} + P_{sw\,Ns})}{P_{cond\,S} + P_{sw\,S}} = \frac{P_{cond\,S}\frac{N}{B} + \frac{P_{sw\,S}}{N^{A-1}}}{P_{cond\,S} + P_{sw\,S}} \quad (3)$$

In case of 2 serial inverters coefficients by using MOSFETs from Cree C3M0025065J1 for 650V and C3M0032120J1 for 1200V are:

$$B = 1.84, A = 1, N = 2, \frac{P_{cond\,N}}{P_{cond\,S}} = \frac{1.08 * P_{cond\,S} + P_{sw\,S}}{P_{cond\,S} + P_{sw\,S}} \quad (4)$$

Therefore, there is almost no difference in total power losses and doubled number of switching devices. This approach might be effective to utilize GaN and Si MOSFET with relatively low blocking voltage in high input voltage applications. Also it could be useful in case of distributed areas of PE or modular structure. However, the advantage of the method is not evident if SiC devices are selected, and it should be investigated deeply. Usually, their blocking voltage is high enough to cover the typical voltage range for EV application (<900V) without voltage sharing. Moreover, the method requires extra voltage control and balancing for each stage.

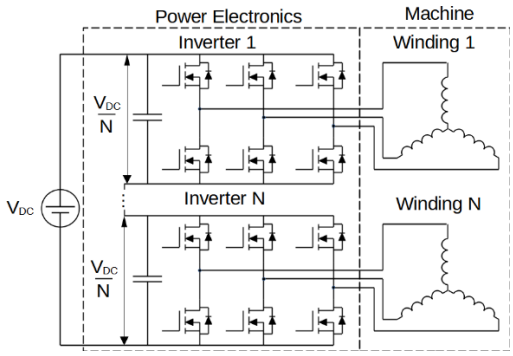


Figure 33 – Serial connection of 3-phase 2-level VSI

Topologies with the increased number of phases or parallel/serial inverters are also able to operate with interleaving to reduce the current through the DC-link capacitance.

B) 3-level topologies

Today 3-level topologies are frequently used in AC/DC power devices in automotive and industrial applications. Serial connection of MOSFETs reduces their maximum blocking voltage required, and the total resistance and conduction losses also become lower. This topology has lower output Total Harmonic Distortion (THD) and lower machine losses which could be valuable for reducing machine dimensions. At the same time, the higher numbers of switches and connections between switching groups complicate the arranging of the inverter structure inside the limited volume. The exact result of such a "trade-off" is not studied yet and needs further investigation. Lower electric stress on the machine's winding insulation could be an advantage for high power and high voltage motor drives, but it is probably not an issue for EV traction application.

Nevertheless in this study a number of 3 level inverter topologies are evaluated to demonstrate their advantages over the typical 2-level system. Simple NPC (with diodes), active NPC (ANPC), and T-connected NPC (TNPC) represents 3 level inverters (see their schemes in Figure 34).

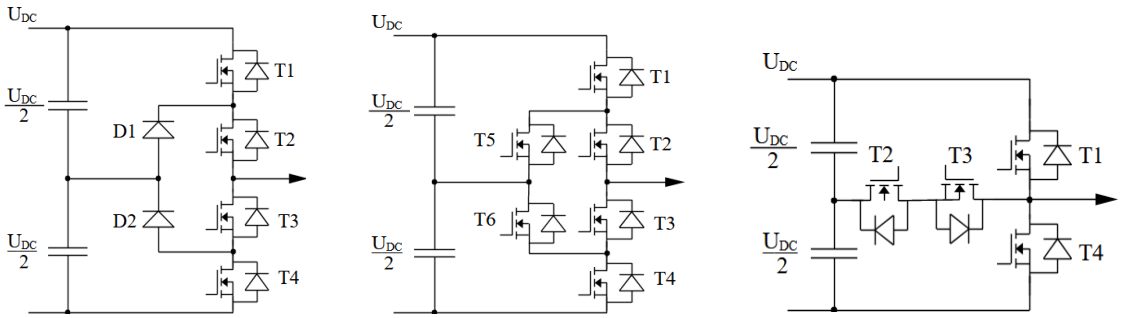


Figure 34 - 3-level topologies (from the left NPC, ANPC, and TNPC)

C) Current source inverters (CSI)

Some studies present the CSI as a good candidate to be exploited in IMD[21, 23] because of the different type of main energy store component (inductors instead of capacitors) that has a wider range of operating temperature, sinusoidal output voltage, and lower CM EMI[23]. The prototype is built and tested to proof the theory. Moreover, if common mode and differential mode filters are included in the design model, the total component volume and relative costs are less for CSI type [82]. Conversely, CSIs are featured with higher inverter power losses and a greater number of power elements [80]. Therefore, such a structure requires a better cooling system and more space for power electronics to maintain the operating conditions.

Similar to 3-level inverters, CSI might be beneficial for total IMD characteristics even with worse inverter parameters, and the influence of each part on the final result could be additionally studied in further research.

Conclusion

Single 2-level 3-phase VSI topology is selected for the analysis due to several reasons:

- Low DC voltage does not allow 3-level topology to show its advantages because the current THD and insulation stress of the machine winding is still at the acceptable level. Most novel MOSFETs have enough high blocking voltage to operate without voltage sharing in EV traction applications.
- Advantages of CSI also are not clearly applicable for low voltage applications; therefore, the topology is not included in consideration for further analysis.
- Multi-phase and parallel/serial inverters can show comparable results to the traditional topology, but, generally, the power density of these solutions is lower. Therefore, in the absence of requirements for fault tolerance or non-standard machine structure, simple topology looks like a preferable choice. At the same time, IMD parameters are subject to individual requirements and design. Thus, final values might be different under certain conditions.
- Further research is required to evaluate the achievable levels for IMD power densities with various non-typical topologies (3-level and CSI) as they have the opposite effect on the inverter and the machine. It is also interesting to compare the performances of single and multi-phase inverters (especially with parallel 3-phase power modules).

3.2 Power switches. Types and characteristics.

In this study, three families of semiconductor power switches are considered as a candidate for the role of a power switch of IMD. They are power modules, discrete MOSFETs with THT package, and discrete SMT MOSFETs package. Dies are not included in the analysis due to the complexity of install process; however, all methods described here could be applied with some modifications to them as well.

To compare different models within the same type of switching devices figure-of-merit (FOM) parameter could be used. Although the parameter provides a rough assessment and does not consider detailed characteristics, it can give a brief review of MOSFETs' performance. The classical equation for FOM of MOSFET proposed in [83] is

$$FOM = R_{ds\,on} Q_g, \tag{5}$$

where $R_{ds\,on}$ is drain-source on-state resistance to present conduction losses, Q_g is total gate charge to indicate switching speed and gate driver requirements. However, another set of parameters would be a preferable option for high-power electronics as the maximal possible output power of the inverter depends on the maximum current $I_{dc\,max}$, drain-source voltage $V_{dc\,max}$, and junction-case thermal resistance Θ_{JC} of MOSFET. In general, the continuous drain current presented in datasheets correlates with $R_{ds\,on}$, but it takes into account also current capabilities of the MOSFET inner connection. For example, SCTL90N65G2V and SCTH90N65G2V-7 have the same die and different packages. As a result, values of $R_{ds\,on}$ are very close, but $I_{dc\,max}$ is different. Thermal properties of MOSFET presented by junction-case thermal resistance are also always stated in its datasheet. Gate characteristics (i.e., input capacitance, total gate, and gate-drain charges) are not so important as modern integrated gate drivers provide wide ranges for their output current. However, if several MOSFETs are connected in parallel or a power module is used, gate charges become too large, and the maximum gate current reaches tens of amps. Further increase of current is a challenging task with standard solutions.

The proposed FOM for power MOSFETs could be calculated according to the following equation:

$$FOM = \frac{I_{dc\,max} V_{dc\,max}}{Q_g \Theta_{JC}}, \tag{6}$$

Drain-source voltage might be excluded from the equation if the voltage is limited by some requirements and cannot be changed (current-focused FOM). It could be helpful to add total volume $\mathcal{V}_{inv}$ for power modules as most of them have different types of packages

(volume-focused FOM). Total gate charge could be excluded from the expression if the gate circuit is considered ideal without limits for gate current. In that case, FOM correlates with achievable output power only (output-focused FOM).

$$FOM_{Vol} = \frac{I_{dc\,max} V_{dc\,max}}{Q_g \Theta_{JC} \mathcal{V}_{inv}}, FOM_{current} = \frac{I_{dc\,max}}{Q_g \Theta_{JC}}, FOM_{out} = \frac{I_{dc\,max} V_{dc\,max}}{\Theta_{JC}} \quad (7)$$

A) Power modules

Power modules are high power density switching devices that use large dies or parallel dies to achieve high values for output current. Advanced technological processes and standardized approaches in industrial manufacturing enable high heat transfer performance, good reliability, and repeatability.

The significant drawback of power modules is the difference in packages and pin layouts for different manufacturers or modules' families of the same manufacturer. Attempts to achieve unification could be noticed only in dimensions and attachments of the module's heat sink in order to use the same cold plate for different modules (see Figure 35).

Figure 35 – Power modules with 106×62 form-factor (pin layout is completely different).

In general, power modules are unsuitable for parallel connection without additional measures due to difficulties with current balancing. Relatively large dimensions cause high parasitic inductances in gate circuits and high-power lines and, therefore, current inequality. If power scaling is required with power modules, a parallel connection is usually created on the system (inverter) level. Parallel operation of power modules is not considered in the analysis.

Although the current study addressed the role of discrete SMT MOSFET in IMD design, the analysis includes several recently designed power modules for comparison. These modules represent the best-achieved values in output current and package dimensions for all leading manufacturers in the market. Most modules include two switches in a "half-bridge" structure, and two modules are full 3-phase 2-level inverters. Before, 3-phase modules had significantly lower output current (less than 50A) due to small die areas; now, the current capabilities are enough to use the modules in small traction applications. These modules are strong competitors to other designs within their power limits.

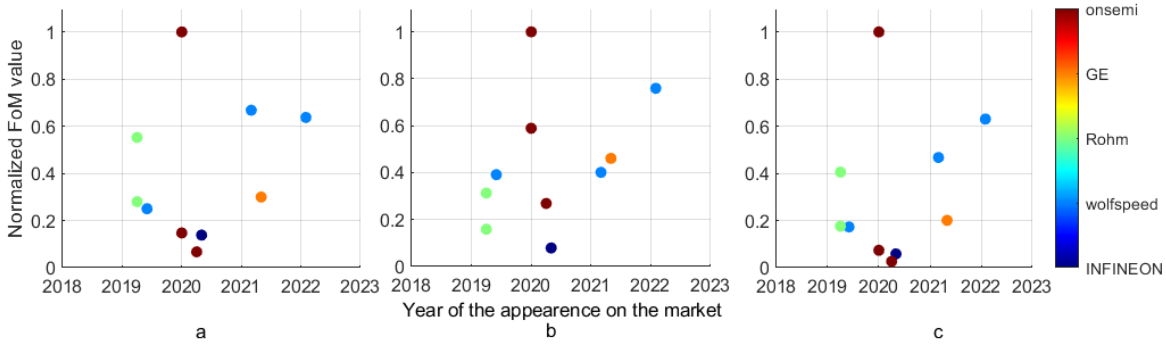


Figure 36 – Different FOM variants for power modules (a – FOM, b – FOM_{Vol}, c – FOM_{out})

The recent development of SiC modules increases both power density and maximum output current (see Figure 36). As mentioned earlier, the modules produced by Wolfspeed show excellent figures for maximum output power and thermal performance; moreover, the improvement of module's characteristics has been steady in recent years. The top position in FOM rating belongs to the module MSCSM120AM02CT6LIAG by Onsemi due to the lowest thermal resistance (due to AlN substrate) and the second rating in the maximum output current. Detailed parameters of power modules considered are listed in Table 7

Table 7 – Power modules included in comparison analysis

№	Name	Year	$R_{ds\,on}$, mOhm	$I_{dc\,max}$, A	V_{dc}, V	C_{ISS}, nF	Q_g, μC	Θ_{J-C}, K/W	T_J, °C	Length, mm	Width, mm	Height, mm	Weight, g
Wolfspeed													
1	CAB760M12HM3	2.2022	1.33	1015	1200	79,4	2,72	0,068	175	110	65	12,2	180
2	CAB530M12BM3	3.2021	2.67	719	1200	39,6	1,36	0,065	175	103,5	60,4	30	300
3	CAB450M12XM3	6.2019	2.6	450	1200	38,0	1,33	0,11	175	80	53	15,75	175
INFINEON													
4	FF6MR12KM1P	5.2020	5.8	250	1200	14.7	0.49	0.181	150	106	61	30,5	340
Onsemi													
5	MSCSM120AM02CT6LIAG	1.2020	2.1	947	1200	36.2	2.78	0,04	175	108	62	16	320
6	*MSCSM120TAM11CTPAG	1.2020	8.4	251	1200	9	0.69	0,144	175	108	62	11,5	250
7	*MSCSM70TAM10CTPAG	4.2020	7.5	238	700	9	0.43	0,222	175	108	62	11,5	250
Rohm													
8	BSM600D12P3G001	4.2019	1.8	576	1200	31	1.5	0,06	175	152	62	20,8	300
9	BSM400D12P3G002	4.2019	4.5	400	1200	17	1.1	0,096	175	152	62	20,8	300
GE Aviation													
10	GE12047CCA3	5.2021	3.1	475	1200	29.3	1.25	0.1	175	89,3	51,2	14,8	120

* 3-phase module

B) Through-hole pin SiC MOSFETs

SiC MOSFETs could be found in wide ranges of drain current and blocking voltage on the market to provide engineers with freedom in balancing required performance, losses, and cost. Generally, every manufacturer has series for 650V/900V, 1200V, and 1700V with different die area that gives scaled values for $R_{ds\,on}$, inner parasitic capacitances, and Θ_{J-C}. Devices with the highest figures for the current are selected for the analysis to increase power density of the system. Maximum drain voltage is limited by 1200V to target typical requirements for EV traction drivers. It is possible to use MOSFETs with higher blocking voltage, but they have worse dynamic characteristics and higher $R_{ds\,on}$. All MOSFETs selected for the analysis are implemented with package TO-247-4 (or its modifications) due to improved switching behaviour by comparison with classical TO-247, where the gate circuit shares the source pin with power output. Although 4-pins packages were rare several years ago, all new modifications are presented in TO-247-4 today.

In total, 9 types by 7 companies are selected, and their parameters are presented in Table 8. Despite the leading position in the production of power modules, Wolfspeed does not have relatively new devices in the TO-247-4 package, and their most advanced sample was presented in 2019. Therefore, its characteristics do not impress when compared with new devices of other companies. Cascode devices by UnitedSiC offer significantly lower value for both $R_{ds\,on}$ and Θ_{J-C}. In contrast to other MOSFETs the maximum current is limited by bondwires at 120A and case temperature of 125℃. New chinese company PNJ semi produces MOSFET P3M12017K4 with interesting combination of characteristics. The state-of-art is IMZA120R007M1H by Infineon, which has characteristics similar to cascode devices and almost doubled maximum drain current. It would be worth mentioning that it is almost impossible to reach such a high current due to the incredible amount of generated heat (about 700W at 25℃). The maximum drain current could be expressed as:

$$I_{D\,MAX\,RMS}^2 R_{ds\,on} + A \cdot I_{D\,MAX\,RMS} = \frac{T_{J\,MAX} - T_{COOLANT}}{\theta_{J-C} + \theta_{C-Amb}} \tag{8}$$

$$I_{D\,MAX\,RMS} = -\frac{A}{2R_{ds\,on}} + \sqrt{\frac{A^2}{4R_{ds\,on}^2} + \frac{T_{J\,MAX} - T_{COOLANT}}{R_{ds\,on}(\theta_{J-C} + \theta_{C-Amb})}}$$

$$A = \begin{cases} \frac{2F_{SW}E_{SW\,T\,RATED}}{\pi I_{D\,RATED}}, & PWM\ AC\ current \\ 0, & Continuous\ current \end{cases}$$

According to the experimental results, the cooling system with sufficient performance includes 2-phase direct cooling (required heat transfer coefficient is about 30 $\mathrm{W/cm^2K}$).

Reasonable range for drain current for typical applications is below 40-50% of maximum value (see Figure 37).

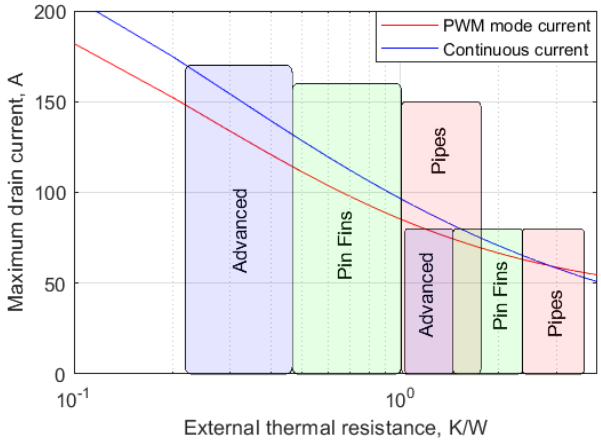


Figure 37 – Maximum current vs case-ambient thermal resistance (left group – with AlN heat spreader, right group – mica insulation pad/grease, MOSFET - IMZA120R007M1H, flowrate 1GPM)

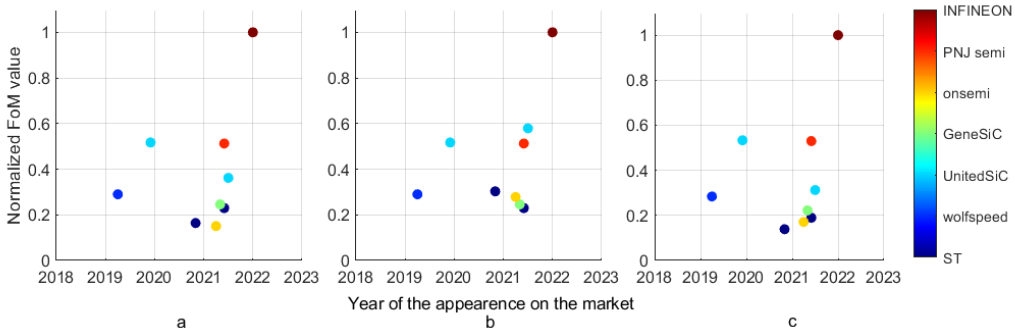


Figure 38 - Different FOM variants for THT MOSFETs (a – FOM, b – $FOM_{current}$, c – FOM_{out})

The set of FOMs for THT devices, including FOM, $FOM_{current}$, and FOM_{out} is presented in Figure 38. Volume-related FOM_{Vol} is not presented as the package's parameters are almost identical for all devices.

Developing the most powerful THT devices focuses on increasing the die area and improving inner connections as it boosts current capabilities and reduces thermal resistance. Addition attention to this package could be obtained if developers implement embedded insulation for the thermal pad (similar to advanced isolation by Infineon for IGBT packages).

Table 8 – THT MOSFETs included into analysis.

№	Name	Year	$R_{ds\ on}$, mOhm	$I_{dc\ max}$, A	V_{dc}, V	C_{ISS}, nF	Q_g, μC	Θ_{J-C}, K/W	T_J, °C	Package
ST Microelectronics										
1	SCTWA90N65G2V-4	11.2020	18	119	650	3.38	0.157	0.31	200	HiP247-4
2	SCTWA70N120G2V-4	6.2021	21	91	1200	3.54	0.15	0.32	200	HiP247-4
PNJ semi										
3	P3M12017K4	6.2021	17	151	1200	7.29	0.27	0.19	175	TO-247-4
Wolfspeed										
4	C3M0016120K	4.2019	16	115	1200	6	0.21	0. 27	175	TO-247-4
Infineon										
5	IMZA120R007M1H	1.2022	7	225	1200	9.17	0.22	0.15	175	PG-TO247-4-STD-T3.7
Cascode UnitedSiC										
6	UF3SC120009K4S	12.2019	8.6	120	1200	8.5	0.23	0.15	175	TO 247-4L
7	UJ4SC075006K4S	7.2021	5.9	120	750	8.31	0.16	0.16	175	TO 247-4L
GeneSiC Semiconductor										
8	G3R20MT12K	5.2021	20	100	1200	5.8	0.18	0.3	175	TO 247-4
Onsemi										
9	NTH4l015N065SC1-D	4.2021	12	142	650	4.79	0.28	0,3	175	TO 247-4L

C) Surface-mount discrete MOSFET

The number of manufacturers producing SiC MOSFET in SMT packages has risen since their first appearance in 2015. Despite the outstanding characteristics of early devices compared with the Si ones, nowadays, these MOSFETs are obsolete as many companies have developed new generations with significantly improved characteristics. In details important characteristics of many most advantageous serial SiC MOSFETs are presented in Table 9. Surface-mount SiC MOSFETs are presented on the market with wide ranges of commutated current and maximum drain voltage (standard values are 650V, 900V, 1200V, 1700V). Trends are to reduce $R_{ds\,on}$ and Θ_{J-C} by increasing the die area and inner connection techniques. At the same time, developers started to use more compact packages to reduce the area occupied by the chip. ST Microelectronics presented SCTL90N65G2V in PowerFLAT 8x8 HV package, offering a twice smaller and significantly thinner package that can be useful in compact, low-current applications. Although the die can conduct high current (SCTH90N65G2V-7 in TO-263-7 package has maximum current 116A), package capabilities limit the value by 40A. In 2022 Onsemi developed NTBL045N065SC1 in package H−PSOF8L, which has a larger thermal pad area, very short pin length, and reduced package thickness. MOSFETs in TO-263-7 package suffer the same problem as TO-247 MOSFETs when high drain current is mostly virtual as it requires complex thermal management to maintain case temperature closed to ambient value and, therefore, avoid current reduction (Figure 39 illustrates current derating due to limited performance of the cooling).

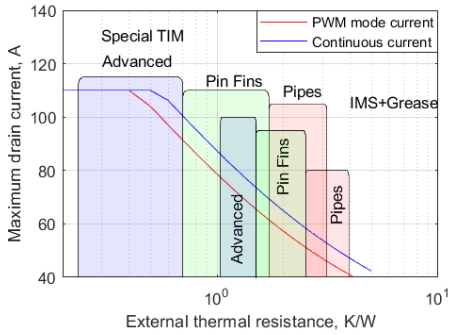


Figure 39 - Maximum RMS current vs case-ambient thermal resistance (left group – with AlN heat spreader, right group – IMS PCB, MOSFET - SCT011H75G3AG) and appropriate cooling techniques (flowrate 1GPM).

With typical cooling solutions (IMS PCB with/without thermal grease and a single phase cold plate), it is hard to achieve more than 50-60A RMS current per MOSFET even at 25°C of ambient temperature.

Some companies presented package modifications with straight leads to use with non-

standard PCB structures (vertical or elevated control boards with gate traces).

The market of SiC SMT MOSFETs is a dynamic and rapidly developing field with both steady improvements of existing technologies and new approaches. Every 1-2 years new series of semiconductor devices become available and push the boundaries of PE power density (see continues rise of FOMs over last 7 years, Figure 40). Engineers and designers of PE have a significant advantage in using SMT power switches as all MOSFETs can be replaced by other types (for example, better ones) without modification of PCB layout. The only condition is to be compatible with the gate circuit due to higher (in most cases) gate capacitance of novel MOSFETs.

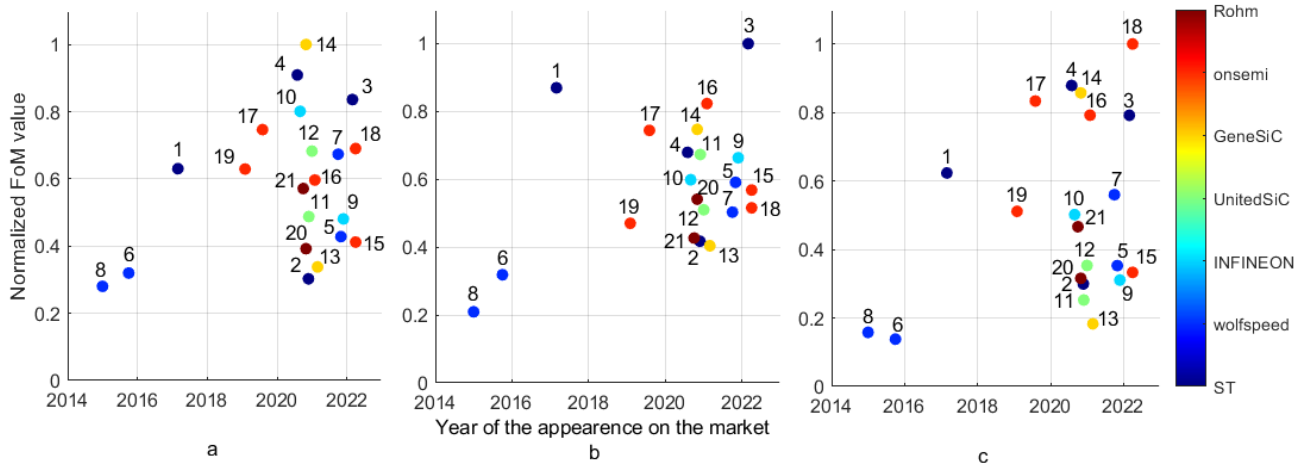


Figure 40 - Different FOM variants for SMT MOSFETs (a – FOM, b – $FOM_{current}$, c – FOM_{out})

Table 9 - SMT MOSFETs included into analysis.

№	Name	Manufacturer	Year	$R_{ds\,on}$, mOhm	$I_{dc\,max}$, A	V_{dc}, V	Θ_{J-C}, K/W	C_{ISS}, nF	Q_g, nC	T_J, °C	A_{HS}, mm^2	Package
1	SCTH90N65G2V-7	ST Microelectronics	3.2017	18	116	650	0,31	3.38	157	175	53,3	H2PAK-7
2	SCTL90N65G2V		12.2020	18	40	650	0,16	3.38	157	175	31,7	PowerFLAT 8x8
3	SCT011H75G3AG		3.2022	11	110	750	0,23	3.83	144	175	53,3	H2PAK-7
4	SCTH70N120G2V-7		8.2020	21	90	1200	0,32	3.54	150	175	53,3	H2PAK-7
5	C3M0025065J1	Wolfspeed	11.2021	25	80	650	0,46	2.98	110	150	61,9	TO-263-7L XL
6	C3M0065090J		10.2015	65	35	900	1,1	0.76	30	150	44,6	TO-263-7
7	C3M0032120J1		10.2021	32	68	1200	0,45	3.42	110	150	61,9	TO-263-7L XL
8	C3M0075120J		1.2015	75	30	1200	1,1	1.35	50	150	44,6	TO-263-7
9	IMBG65R022M1H	Infineon	12.2021	22	64	650	0,5	2.29	67	175	51,0	PG-TO263-7-12
10	IMBG120R030M1H		9.2020	30	56	1200	0,38	2.29	63	175	51,0	PG-TO263-7-12
11	UF3SC065030B7S	Cascode UnitedSiC	12.2020	27	62	650	0,54	1.5	43	175	44,6	D2PAK-7
12	UF3SC120040B7S		1.2021	35	47	1200	0,54	1.5	43	175	44,6	D2PAK-7
13	G3R60MT07J	GeneSiC Semiconductor	3.2021	60	44	750	0,69	0.95	47	175	44,6	TO-263-7
14	G3R30MT12J		11.2020	30	85	1200	0,3	3.86	118	175	44,6	TO-263-7
15	NTBL045N065SC1	Onsemi	4.2022	33	73	650	0,43	1.87	105	175	55,2	H−PSOF8L
16	NVBG015N065SC1		2.2021	12	145	650	0,3	4.69	283	175	52,0	D2PAK−7L
17	NVBG020N090SC1		8.2019	20	112	650	0,31	4.42	200	175	52,0	D2PAK−7L
18	NTBG014N120M3P		4.2022	16	104	900	0,33	6.31	337	175	52,0	D2PAK−7L
19	NVBG040N120SC1		2.2019	40	60	1200	0,42	1.79	106	175	52,0	D2PAK−7L
20	SCT3030AW7	Rohm	11.2020	30	70	650	0,44	1.53	104	175	52,0	TO-263-7L
21	SCT3040KW7		10.2020	40	56	1200	0,44	1.34	107	175	52,0	TO-263-7L

3.3 Comparison analysis of MOSFETs with different packages.

A) Losses calculation and thermal model

Designers of PE have to operate power switches at the edge of their thermal stability if the high power density is prior target. Proper assessment of the MOSFETs' operational point and heat transfer is crucial to maintaining the junction temperature below the rated value. At the same time, the number of MOSFETs should be minimal to reduce weight and dimensions.

The total dissipation of a single device can be obtained with the sum of conduction and switching losses

$$P_{MOSFET} = P_C + P_{SW} = I^2_{\mathrm{DS}\,rms} R_{ds\,on}(Tj, I_{DS}) + F_{sw} \frac{E_{SW\ tot\ rated}}{\pi} K_{Tj} K_{Vdc} K_I K_{Rg}, \quad (9)$$

where $I_{\mathrm{DS}\,rms}$ is RMS current of a single MOSFET, $E_{tot\ rated}$ – total switching losses at the operation point specified in the datasheet, K_x are scaling coefficients which value depends on junction temperature (for K_{Tj}), input DC-link voltage (for K_{Vdc}), drain current (for K_{Ids}), and external resistance of gate circuit (for K_{Rg}). Usually, all figures and charts regarding losses, temperature influence, and drain current are shown at one or several specified operating points in the datasheet to ease the analysis if many parameters change simultaneously. MOSFET's parameters, measured at this operating point, have an index "rated" in their description

There is no need to calculate reverse recovery losses and recharge losses of output capacitance separately or distinguish them from total switching losses, because a body diode of the same MOSFET is used to obtain experimental values of switching losses specified in datasheet.

Only 2-level 3 phase topology with sinusoidal PWM is considered in the analysis, therefore, RMS current of each switching group is equal to a half of the maximum phase current

$$I_{\mathrm{DS}\,RMS\,G} = \frac{I_{\mathrm{PH}\,MAX}}{2} \quad (10)$$

Dead-time related losses also are not included (MOSFETs generate all conduction losses). For the majority of devices voltage drop on the $R_{ds\,on}$ in reverse conduction is lower than forward voltage of body diode (especially for negative biased gate voltages) within reasonable values of drain current, therefore, diode conduction losses are not included in this model. All parallel devices are considered equal with an even share of drain current, and the drain current of single devices is calculated as follows:

$$I_{\mathrm{DS}\,rms} = \frac{I_{\mathrm{DS}\,RMS\,G}}{N_{PPG}} \quad (11)$$

Detailed discussion on issues of MOSFETs parallel operations is added at the end of this chapter.

Drain-source channel resistance $R_{ds\,on}$ depends on the $V_{GD\,max}$, T_J, I_{ds}, but $V_{GD\,max}$ is fixed to the datasheet rated values and excluded from the analysis. Other parameters change their values with every iteration, and they are taken into account as explained:

$$R_{ds\,on}(T_J, I_{ds}) = R_{ds\,on25}\left(1 + KR_{T_J}(T_j - T_{jLT})\right) \cdot KR_I \tag{12}$$

$$KR_{T_J} = \frac{Rn_{ds\,on\,TjHT} - 1}{T_{jHT} - T_{jLT}}, KR_I = \frac{aI_{DS\,RMS} + b}{R_{ds\,on25}}$$

where $R_{ds\,on25}$ - drain-source channel resistance at 25°C, $Rn_{ds\,on\,TjHT}$ – normalized value (with respect to $R_{ds\,on25}$) of drain-source channel resistance in the high temperature (T_{jHT}), T_{jLT} – maximum junction temperature where $Rn_{ds\,on\,Tj}$ is equal to 1 (or $R_{ds\,on}$ is equal to $R_{ds\,on25}$). The normalized version is used as it is the most popular representation of the relation $R_{ds\,on}(T_j)$ in datasheets. Coefficients a, b of KR_I extracted from the datasheet for the current range 10A-60A where it could be approximated as a linear function with acceptable error. Higher equation order might be used as the curve becomes non-linear for higher current.

Coefficients for switching losses could be calculated as linear, quadratic or power approximations depending on the shape of the curve:

$$K(x) = \begin{cases} \left(\frac{V_{DC}}{V_{DCrated}}\right)^a, & for\ V_{dc} \\ \frac{ax^2 + bx + c}{E_{total\,rated}}, & for\ I_{dc} \\ \frac{ax + b}{E_{total\,rated}}, & for\ R_g, T_j \end{cases} \tag{13}$$

where a, b, and c – parameters extracted from MOSFET's datasheet.

As mentioned before, usually gate circuit does not limit the performance of MOSFET due to the high ratings of modern gate drivers. The most popular upper limit of output current for "single chip" gate drivers is about 25-30A, which is the maximum total gate current for analysis. It is assumed that $\frac{dV_{DS}}{dt}$ is directly proportional to the rate of charging of drain-gate charge $\frac{dQ_{GD}}{dt}$ and Miller plateau's voltage V_{GDMill} does not change during this process. Therefore, the gate current is constant at this moment, and it determines the rise time t_{rise}

$$I_{G\,Miller} = \frac{Q_{gd}}{t_{rise}} = \frac{V_{GDMax} - V_{GDMill}}{R_{g\,inner} + R_{g\,ext}} \tag{14}$$

In the analysis t_{rise} is an input parameter (initial value is 10ns) as it is significant for EMI characteristics of the inverter[84], although gate current itself might be used as an input

parameter.

The relationship between the total maximum gate current I_{GTotal} and the number of parallel transistors could be expressed as follows:

$$I_{Gtotal} = N_{PPG} \frac{V_{GDMax} - V_{GDMin}}{R_{g\ inner} + R_{g\ ext}} \leq 30A \tag{15}$$

Total gate current increases I_{Gtotal} with the number of parallel devices in a group and might reach the limit at some point. Further increase in the number of devices leads to the increase of gate resistance $R_{g\ ext}$ in order to maintain the current at the same level. With higher gate resistance charging current $I_{G\ Miller}$ becomes smaller, and t_{rise} , in opposite, becomes higher. So, the current limitation of gate driver might be a reason for higher switching losses in case of large numbers N_{PPG}.

For some devices high inner resistance $R_{g\ inner}$ and significant value of gate-drain charge Q_{gd} does not allow a driver to charge C_{gd} fast enough to reach the initial value of the rise time. For such devices the initial value of external gate resistance $R_{g\ ext}$ is set to 0, and switching time is calculated with the new initial $R_{g\ ext}$. External resistor $R_{g\ ext}$ for each MOSFET is calculated differently with respect to value of gate current:

$$R_{g\ ext} = \begin{cases} N_{PPG} \dfrac{V_{GDMax} - V_{GDMin}}{I_{GtotalMAX}} - R_{g\ inner}, & I_{Gtotal} = 30A \\ \dfrac{t_{rise}\,(V_{GDMax} - V_{GDMill})}{Q_{gd}} - R_{g\ inner}, & I_{Gtotal} < 30A \\ 0, & I_{Gtotal} < 30A, \dfrac{t_{rise}\,(V_{GDMax} - V_{GDMill})}{Q_{gd}} < R_{g\ inner} \end{cases} \tag{16}$$

The final value $R_{g\ ext}$ is used to calculate coefficient K_{Rg} for switching losses.

Although datasheets for most modern MOSFETs contain all necessary information, documents for older MOSFETs might miss some plots or figures. In that case, default values selected by simplified losses equations are used in the calculation (values are listed in Table 10).

Table 10 – Default values of coefficients for losses calculation

K_{Rg}	K_{Tj},	K_{Vdc}	K_I	KR_{Tj}	KR_I
a=1, b=0	a=0, b=Rated value	a=1.4	a=0, b=1, c=0	$Rn_{ds\ on\ TjHT} = 1$	a=0, b=$R_{ds\ on25}$

The junction temperature of a device consists of ambient temperature T_{amb}, temperature drop between MOSFET's case and junction ΔT_{j-case}, and temperature drop between the case and coolant $\Delta T_{case-hs}$:

$$T_j = \Delta T_{case-hs} + \Delta T_{j-case} + T_{amb} = P_{MOSFET}\left(\Theta_{j-c} + \Theta_{C-hs} + \frac{1}{S_{\text{PCB AREA}} h_{CP}}\right) + T_{amb}, \tag{17}$$

$$\Theta_{c-hs} = \begin{cases} \Theta_{TIM}, & for\ power\ modules \\ \Theta_{Insulation\ pad} + \Theta_{TIM}, & for\ THT\ components \\ \Theta_{PCB} + \Theta_{TIM}, & for\ SMT\ components \end{cases}$$

where S_{hs} is the area of the thermal pad or the baseplate of a device divided by the number of switching groups inside the package (assume that heat evenly spreads across the baseplate), Θ_{c-hs} is the total thermal resistance of layers between the case and the heat sink. Traditional structure with indirect cooling is selected for comparison analysis, therefore Θ_{c-hs} depends on TIM thermal conductivity for power modules. THT components transfer heat through a thermally conductive insulation pad (mica+thermal grease), and for SMT components Θ_{c-hs} depends on both PCB and TIM parameters. PCB also acts as a heat spreader as it has a thermal conductive top layer; therefore, the area involved in heat transfer is larger than the area of the component's thermal pad. Analysis shows that temperature rise (and heat transfer also) of the top copper layer rapidly decreases with distance from the pad (see Figure 41). For 0.07 mm thickness of copper layer and thermal conductivity of prepreg equal to 1 $\frac{W}{m\,K}$ the relative copper temperature drops to about 30% of its maximum value if the distance from the pad exceeds 2 mm.

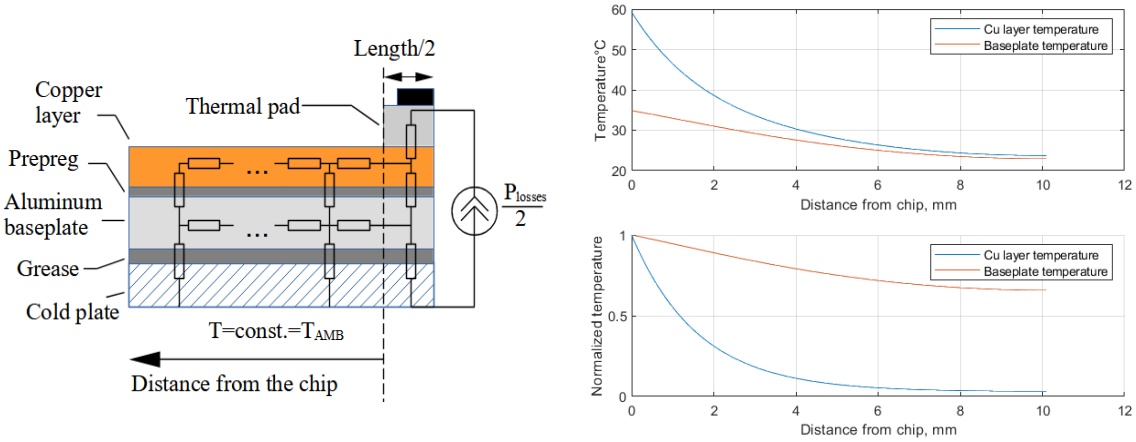


Figure 41 – Thermal model of IMS PCB and relative temperatures of different layers with distance from the thermal pad ($P_{LOSS} = 20W, T_{amb} = 0$°C).

Thick copper layer able to reduce thermal resistance (see Figure 42) to some extent, but its efficiency also depends on the size of PCB (or heat spreader). For the given parameters of thermal stack, prepreg characteristics affect significantly heat conduction capabilities, therefore, the careful selection of the material and manufacturer are highly important here.

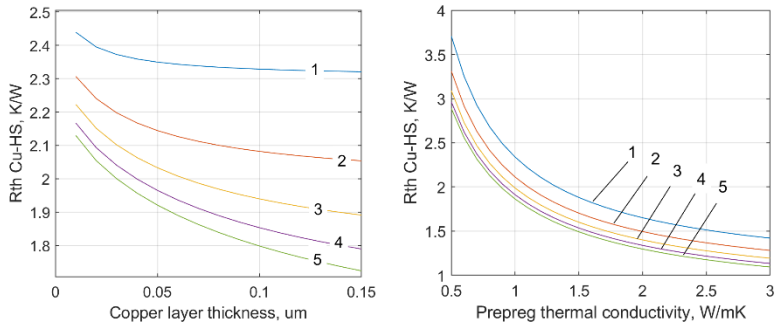


Figure 42 – Effect of heat spreader size (figures are distances between edge of device and edge of PCB), copper thickness, and prepreg thermal conductivity on case-heatsink thermal resistance.

By contrast, temperature spreads along the baseplate surface much further due to the thickness of the metal. Almost all available areas in a 10-15 mm radius around the MOSFET transfer heat to the cold plate. The assumption is made in the analysis of SMT components that heat generated by a group is equally spread across the baseplate area occupied by this group (similar to heat spread in power modules).

As the inverter's area is one of the targets, keeping a small distance between devices is reasonable. For analysis, the distance between two cases is 2mm, and each device uses an extra 1 mm of copper layer on each side of its thermal pad to spread the heat. Other important parameters of thermal interface materials and calculated values of MOSFET's thermal resistances are stated in Table 11, Table 12, and Table 13.

Table 11 – Thermal resistances of SMT MOSFET

Input Parameter	Value	Calculated Parameter	Value
Extra distance from the chip, mm	1	Prepreg (under the pad) thermal resistance $\theta_{Pre\,pad}$, K/W	1.61/3.16
Prepreg thickness, mm	0.1	Pad-baseplate (in vicinity of the pad) thermal resistance θ_{add}, K/W	3.65/4.95
Prepreg thermal conductivity, W/mK	1	Total prepreg thermal resistance, K/W	1.11/1.92
Top copper layer thickness, mm	0.07	Baseplate+grease (per MOSFET) thermal resistance θ_{BP}, K/W	0.47/0.84
Grease thermal conductivity, W/mK	0.73	Heatsink-ambient (per MOSFET) thermal resistance θ_{HS-Amb}, K/W	0.63/1.1
Heat sink size of each MOSFET, mm·mm	(L+10)·(W+2)	Case-ambient thermal resistance θ_{C-Amb} (per MOSFET), K/W	2.22/3.88
Heatsink heat transfer coefficient, W/m^{2}K	0.5	Junction-ambient thermal resistance θ_{single} (per MOSFET), K/W	2.66/4

L, W – length and width of MOSFET's case;

Table 12 – Thermal resistances of THT MOSFET

Input Parameter	Value	Calculated Parameter	Value
Insulation (mica+grease) thermal resistance per area, K/m^{2}W	6.45e-5	Insulation thermal resistance θ_{Ins} , K/W	0.34/0.37
Heat sink size of each MOSFET, mm·mm	(L+10)·(W+2)	Heatsink-ambient (per MOSFET) thermal resistance θ_{HS-amb} , K/W	0.33/0.36
Heatsink heat transfer coefficient, W/m^{2}K	0.5	Case-ambient thermal resistance θ_{C-Amb} (per MOSFET), K/W	0.67/0.73
		Junction-ambient thermal resistance θ_{single} (per MOSFET), K/W	0.88/1.05

Table 13 – Thermal resistances of power modules

Input Parameter	Value	Calculated Parameter	Value
Grease thermal conductivity, W/mK	0.73	Grease thermal resistance θ_{Grease}, K/W	0.039/0.13
Grease thickness, mm	0.1	Heatsink-ambient (per MOSFET) thermal resistance θ_{Grease} , K/W	0.057/0.19
Heatsink heat transfer coefficient, W/m^{2}K	0.5	Case-ambient thermal resistance θ_{single} (per MOSFET), K/W	0.096/0.32
		Junction-ambient thermal resistance θ_{single} (per MOSFET), K/W	0.148/0.54

Heat flux is an important characteristic to estimate requirements on the heatsink, as high heat flux needs a more complicated heatsink structure to maintain equal temperature all over the switching group. Heat flux depends on the area of the device's thermal pad and, in general, could be calculated as follows:

$$Q_{sh} = \frac{P_{total\ part}}{S_{hs}}. \tag{18}$$

The volume (V) and the area (A) of a power module are calculated based on their dimensions from datasheets. The area and the volume of SMT and THT devices include extra space (values are presented in Figure 43) for connections of power buses and gate circuits:

$$A_{SMT} = 6(N_{PPG}(Width + 2mm) + 2mm)(Length + 8\ mm), \tag{19}$$

$$A_{THT} = 6(N_{PPG}(Width + 2mm) + 2mm)(Length + 5mm), \tag{20}$$

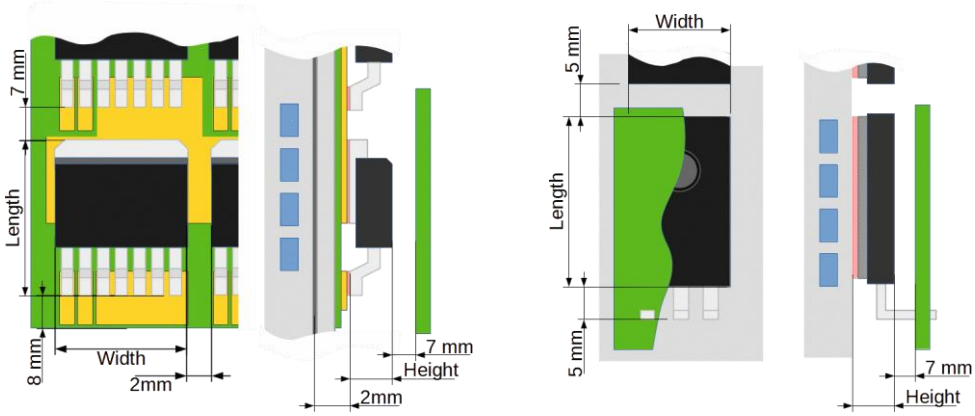


Figure 43 – Layout for SMT (TO-263-7) and THT (TO-247) components

$$V_{SMT} = A_{SMT}(Height + 7mm + 2mm), V_{PTH} = A_{PTH}(Height + 7mm) \quad (21)$$

High junction temperature T_j affects many parameters of MOSFET (mostly drain-source channel resistance, threshold voltage and body-diode charge) and causes the increase of both conduction and switching losses, which, in turn, increase generated heat and junction temperature. The simplified approach assumes that MOSFET always works at the maximum of its junction temperature, and corresponding values are used in the calculation. The simplification gives accurate results when the maximum possible power is the target, but it shows higher losses if the required power is limited; therefore, junction temperature might be less than its maximum value. A multi-iteration algorithm is used to recalculate temperature-dependent coefficients and get accurate results for the whole range of junction temperature (see Figure 44). Initial junction temperature is equal to coolant temperature and is updated every cycle until the difference between the two steps is less than 2ºC. This method helps both detect possible thermal runaway and evade overestimation of conductive losses due to too high expectation of $R_{ds\,on}$. All combinations that led to excessive junction temperature are excluded from the analysis.

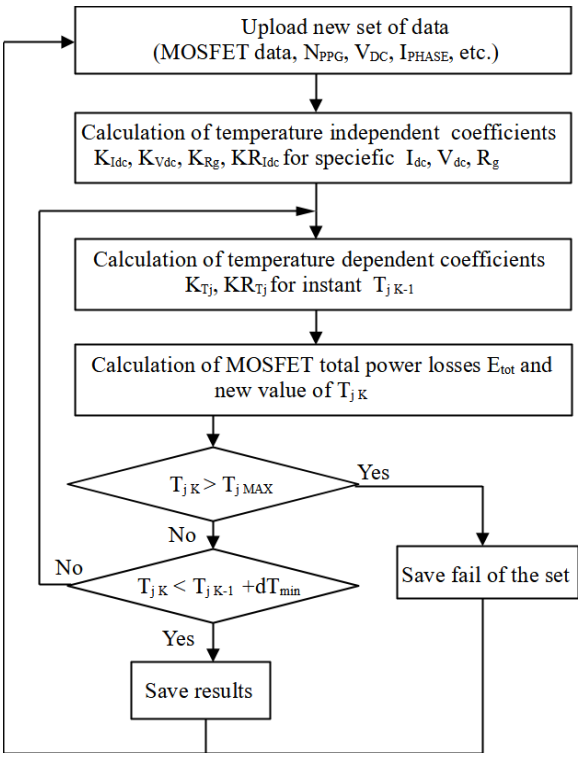


Figure 44 – Flowchart for the calculation of junction temperature

The total weight $W_{module\ total}$ of an inverter with power modules is given by:

$$W_{module} = 3W_{module\ singl}, \tag{22}$$

where $W_{module\ singl}$ is the weight of the power module according to its datasheet.

The total weight W_{SMT} of an inverter with SMT components includes the weight of a 2mm aluminum baseboard as they cannot be used without a heat spreader and can be calculated as:

$$W_{SMT} = 6N_{PPG}W_{part} + A_{SMT} \cdot 2mm \cdot 2.7\frac{g}{cm^2}, \tag{23}$$

where W_{part} is the weight of the single discrete element according to its datasheet.

B) Simulation results

A comparative analysis is carried out to determine the advantages and disadvantages of different package types in terms of losses, occupied space, and generated heat flux.

Results for gate current analysis are presented in Figure 45, Figure 46, and Figure 47. All three types of behaviour of $R_{g\ ext}$ could be noticed there, i.e. with current limitation (t_{rise} changes with the increase of N_{PPG}), without current limitation (t_{rise} is equal to the target value and constant), and with $R_{g\ ext} = 0$ (t_{rise} is constant, but higher than target value). For example, SMT MOSFETs №6, 9-13 can maintain 10 ns switching time for 1-8 parallel devices without reaching the current limit. Devices №8, 20, 21 also stay within the

required values for gate current, but the minimum switching time is only about 26ns and 36ns, respectively. Others reach the threshold of 30A at the number of parallel devices between 2 and 5, and switching time starts to rise after that point.

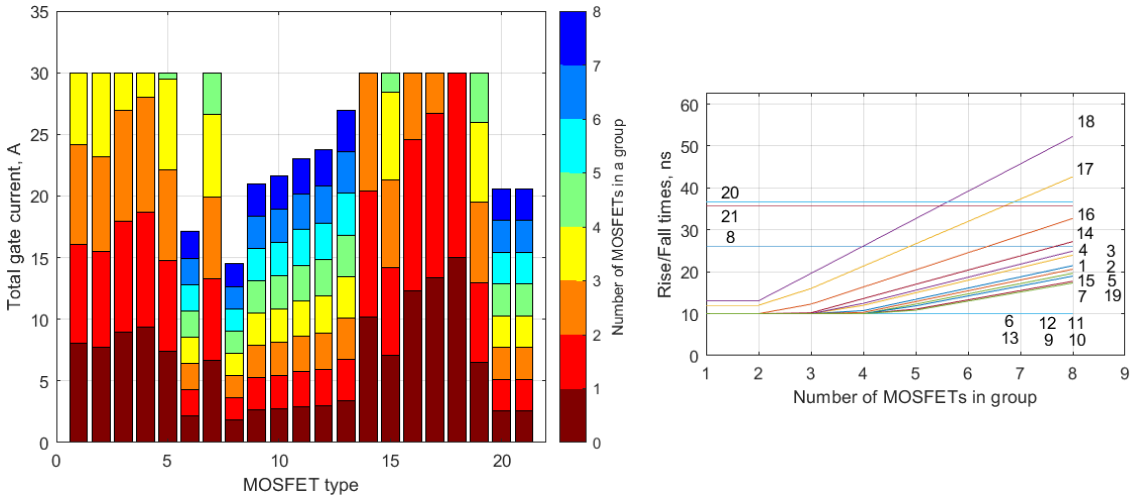


Figure 45 – Total gate current and rise/fall time for different types of SMT MOSFETs

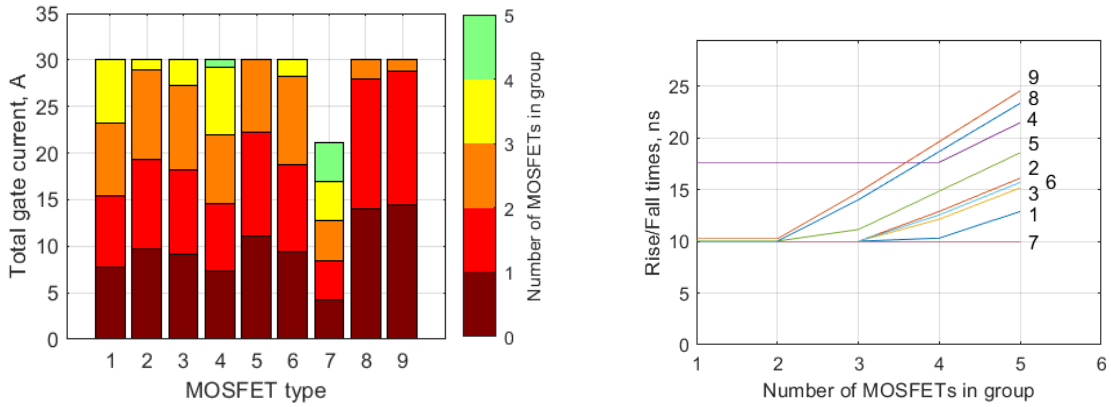


Figure 46 – Total gate current and rise/fall time for different types of THT MOSFETs

The THT MOSFETs show the same pattern with the only difference that more devices reach the maximum gate current threshold due to larger capacitances.

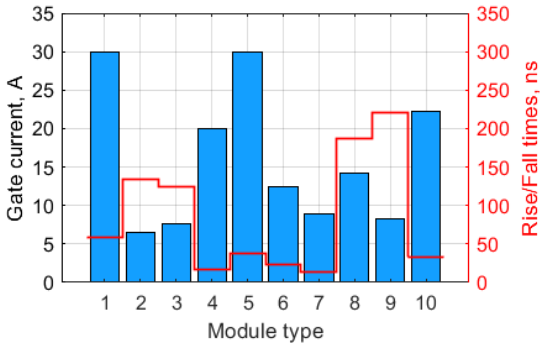


Figure 47 - Total gate current and rise/fall time for different types of power modules

Power modules show quite different results in terms of switching time values. Inner resistance limits switching capabilities significantly as only two of them can reach 30A

level of gate current. At the same time, 4 devices need more than 100ns to change their status.

Weight and dimension preliminary analysis could be done without losses calculation to determine general trends. The maximum number of parallel devices for SMT MOSFETs is set to 8, and the number is 5 for THT MOSFETs. According to the calculations (see Figure 48), occupied area and volume with their maximum numbers of MOSFETs are almost the same for both THT (package TO-247-4) and SMT devices (package TO-263-7).

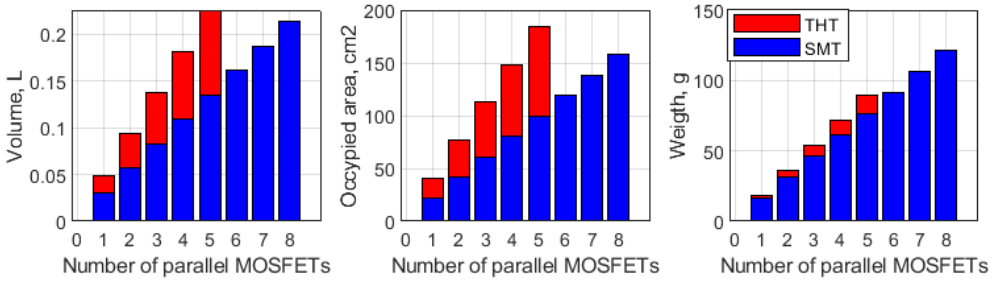


Figure 48 – Results of dimension analysis for whole range of parallel devices

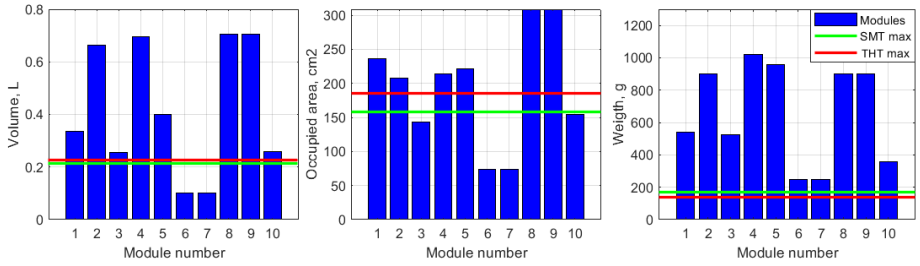


Figure 49 - Results of dimension analysis for power modules (maximum values of SMT and THT devices are added for comparison).

Power modules show significant deviations in dimensions and weight from the average level due to differences in package design and ampacity (see Figure 49). Nevertheless, all of the modules considered are heavier than assembles of discrete MOSFET.

The analysis includes several scenarios with different requirements to observe the capabilities of devices from various points of view.

Scenario 1

Inverter with finite values for maximum phase current $I_{\mathrm{PH}\,MAX}$ and DC-link voltage V_{DC}. Target: evaluate the performance of different packages and compare their occupied areas, weight, and volume.

This scenario includes the analysis with two different ambient temperatures (25°C and 105°C). The thermal model considers temperature parameters of semiconductor devices only; issues of wire conductor overheating are not included and should be addressed separately. System parameters used in the calculation are presented in Table 14; the values

are chosen according to the requirements for typical low-power IMD (for example, [47, 48, 85]). The discrete MOSFETs are connected in parallel, and the number of devices per group is selected according to the device's calculated maximum junction temperature.

TABLE 14 - IMD Parameters for comparative analysis

Parameter	Value
Peak phase current $I_{\mathrm{PH}\,MAX}$, A	200
DC voltage V_{DC}, V	350
Switching frequency F_{sw}, kHz	50
Coolant temperature T_{COOLANT}, °C	25
HTC of the cold plate h_{CP}, W/cm^{2}K	0.5

Normal ambient temperature T_{AMB}=25°C

Individual results for different packages are presented in Figure 50, Figure 51, and Figure 52. For discrete MOSFETs, two sets of data with a different number of parallel devices (minimum and minimum+1) indicate the change in thermal conditions for critical and non-critical operation modes. SMT devices show the highest average junction temperature, with a significant drop (20-60 °C) in the junction temperature for the larger group. The average junction temperature for THT devices is lower by about 30°C than the value for SMT packages and decreases by another 20°C for the larger group. Total losses also decrease due to lower current through a single MOSFET, but the changes vary from type to type and are not as large as the change in junction temperature.

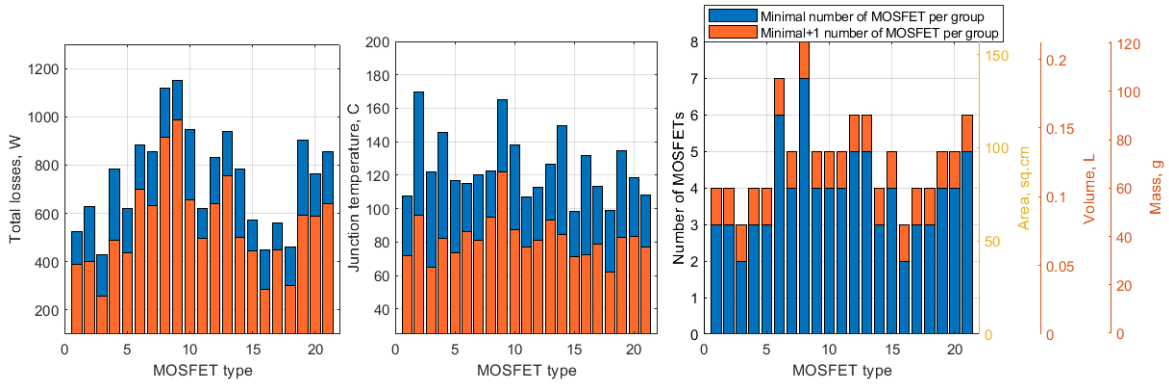


Figure 50 – Total losses and junction temperature of SMT MOSFETs in Scenario 1 (T_{AMB}=25°C)

It is noticeable that the old MOSFET types (SMT №6, 8 were presented in 2015) show worse performance and require a higher number of parallel devices. By contrast, modern devices (THT №5, SMT №3, 18 were presented in 2022) can deliver the same output power with a significantly smaller group size and lower total losses.

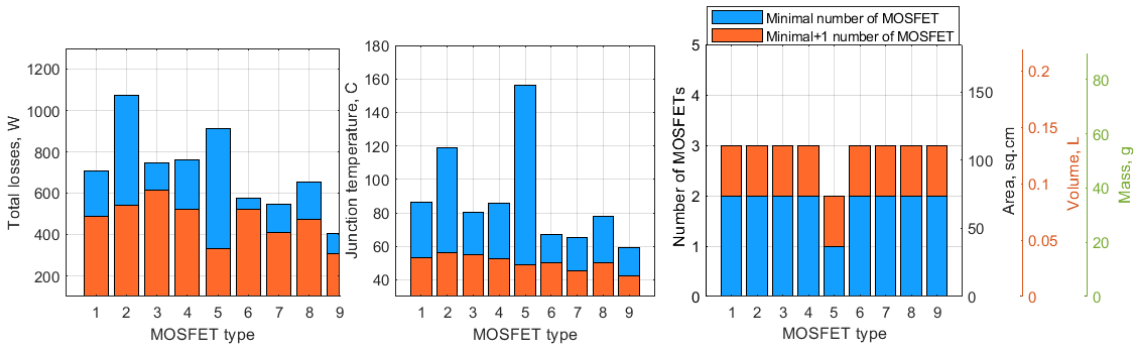


Figure 51 - Total losses and junction temperature of THT MOSFETs in Scenario 1 (T_{AMB}=25°C)

Power modules show the same level of total losses and, in general, low values for junction temperature (presented in Figure 52). Although 3-phase power modules (№6, 7) have the highest junction temperature among other modules and average total losses for a given power level, the compact package gives them an obvious advantage in applications with mass or volume restrictions.

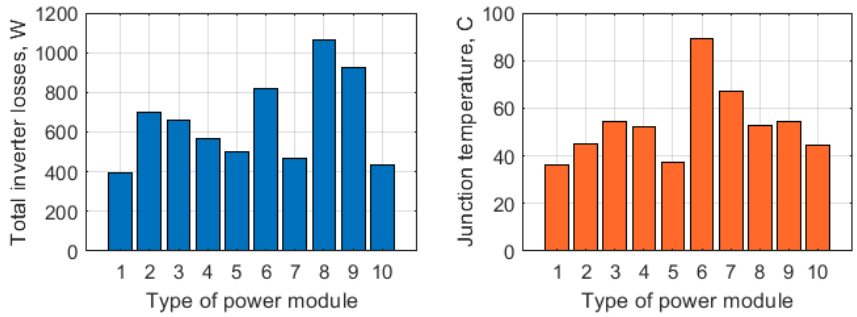


Figure 52 - Total losses and junction temperature of power modules in Scenario 1 (T_{AMB}=25°C)

Radar diagrams in Figure 53 help compare obtained results between packages. Values are normalized by maximum value among all types of devices for each comparative characteristic. The colour area shows the range of values for all components from that group. Also, for each package, three types are selected (the best, the worst options and device with average characteristics) to illustrate the trend of a group, as some devices have significant deviations of parameters from the average value.

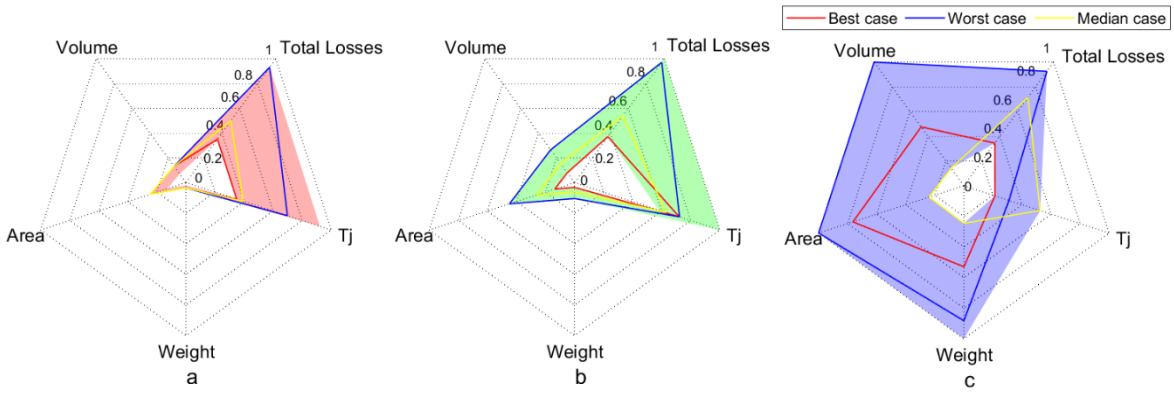


Figure 53 – Normalized analysis results for the minimum number of parallel devices at T_{AMB}=25°C (a – THT, b – SMT, c – power modules)

Another radar diagrams in Figure 54 show the same information for enlarged switching groups of SMT and THT MOSFETs and the same figures for modules. Although there are no noticeable differences in SMT figures, the picture for THT indicates great improvement in both losses and junction temperature (primarily due to the second device in a group of THT №5). At the same time, all dimension-related characteristics still have very low values. In theory, 4-legs THT devices are the best option for this application if other technical and non-electrical characteristics are not considered.

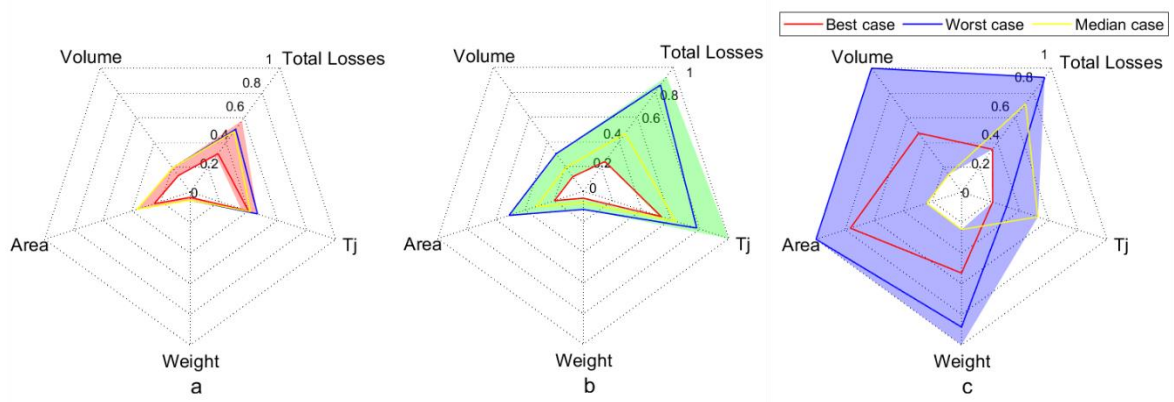


Figure 54 – Normalized analysis results for the (minimum+1) number of parallel devices T_{AMB}=25°C (a – THT, b – SMT, c – power modules)

It is worth mentioning that the analysis considers only mechanical characteristics of packages and PCB (for SMT); therefore, comparisons in volume, area, and weight give too high differences of 5-10 times between power modules and discrete components. Some additional values can be introduced to get adequate values for the characteristics of the inverter (see Table 15). For the given output power of about 50kW, the assessment for additional volume is about 1L, which results in a power density of 30-40 kW/L.

Table 15 – Comparison of inverter's dimensions after modifying additional data.

Parameter	Area, cm^2	Weight, g	Volume, L
Initial average, modules	194	660	0.42
Initial average, SMT	77	59	0.1
Difference, (%)	117(60)	601(91)	0.32(76)
Additional values	1cm*	1000**	0.8+a***
New average, modules	417	1660	1.71
New average, SMT	200	1059	1.07
Difference, (%)	217 (52)	601(36)	0.64 (38)

* - to each side of switching group (for screws, tolerance, etc.)
** - that includes other components, a case and a heatsink
*** - value depends on additional area multiplied by height of package

Modified values do not have such a drastic difference as the initial ones; however, inverters with power modules still have higher average figures in all dimensional characteristics.

Operation under high ambient (coolant) temperature T_{AMB}=105°C

The same analysis is done for ambient temperature T_{AMB}=105°C. The detailed results with calculated total losses and junction temperatures for each package type are presented in Figure 55, Figure 56, and Figure 57.

SMT devices (see Figure 55) show wide ranges of total power losses (from 300W to 900W) and the required number of parallel devices (from 3 to 8). The junction temperature for the majority of devices is above 160°C. Two types of SMT MOSFETs cannot operate under required conditions, and there are no results for them in the diagrams.

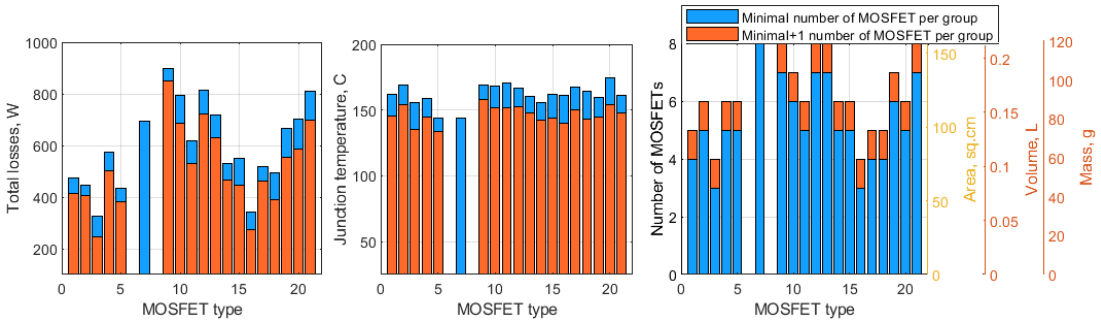


Figure 55 - Total losses and junction temperature of SMT MOSFETs in Scenario 1 (T_{AMB}=105°C)

By contrast, all THT MOSFETs (see Figure 56) can operate at 105°C without reaching the maximum number of parallel devices. Similar to figures at normal ambient temperature, junction temperature of THT devices is lower than those for SMT with comparable amounts of power losses. As most types require only one extra device in parallel, dimensional characteristics change insignificantly. Due to the small minimal number of parallel devices, additional transistor still significantly reduces power losses and junction temperature for some types.

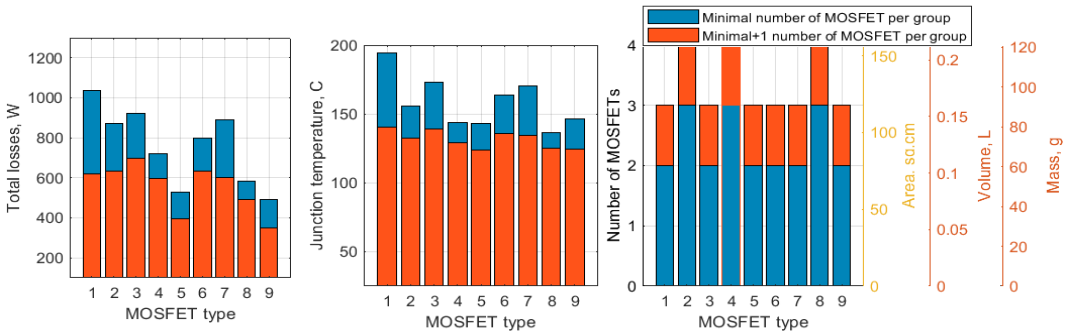


Figure 56 - Total losses and junction temperature of THT MOSFETs in Scenario 1 (T_{AMB}=105°C)

Power modules show acceptable performance under high-temperature conditions, with only two modules unable to operate at T_{AMB}=105°C (results are in Figure 57). Both modules are 3 phase modules, have a smaller heatsink area per a switch, and, thus, have a higher junction temperature at T_{AMB}=25°C. These modules reach the maximum junction temperature much earlier than others.

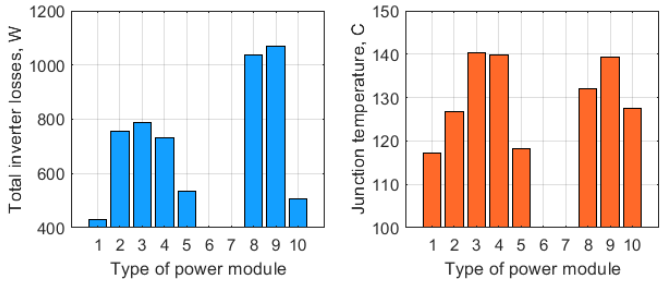


Figure 57 - Total losses and junction temperature of power modules in Scenario 1 (T_{AMB}=105°C)

Normalized radar diagrams (see Figure 58, Figure 59) show almost the same distribution of characteristics and trends as those for normal temperatures. Shaded areas of SMT and THT devices are almost the same, but values become much better for THT if an extra device is added to each switching group.

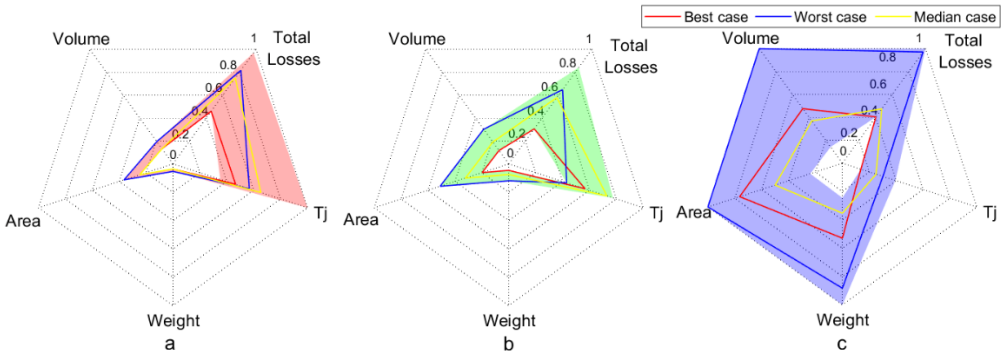


Figure 58 - Normalized analysis results for the minimum number of parallel devices T_{AMB}=105°C (a – THT, b – SMT, c – power modules)

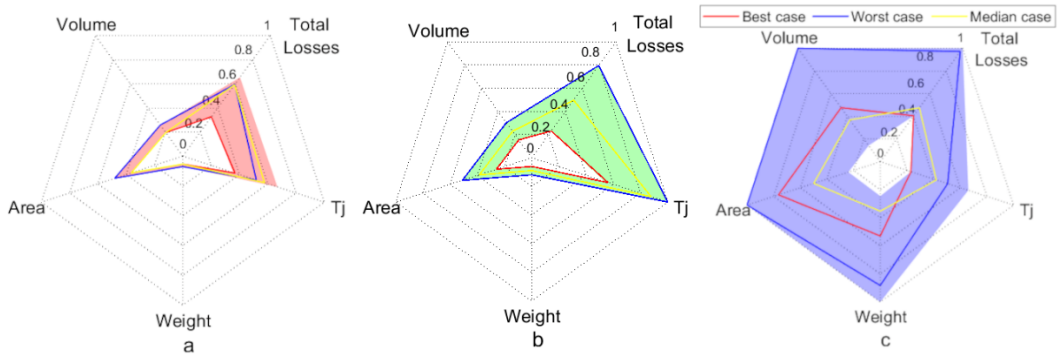


Figure 59 - Normalized analysis results for the (minimum+1) number of parallel devices T_{AMB}=105°C (a – THT, b – SMT, c – power modules)

Graphs of total losses and junction temperature as functions of ambient temperature (see Figure 60) for SMT devices show the maximum ambient temperature for each type (vertical line and the number of MOSFET types). For most types, this temperature is between 120°C and 150°C for given thermal properties of PCB and the heatsink, and only three types can work at 150°C. In the plot P(T_{AMB}), the region shaded with red colour shows the maximum amount of heat that can be transferred from the board in the case of 8 parallel MOSFET with surface temperature 175°C. Total MOSFET's losses must stay below the red line to keep junction temperature below this level.

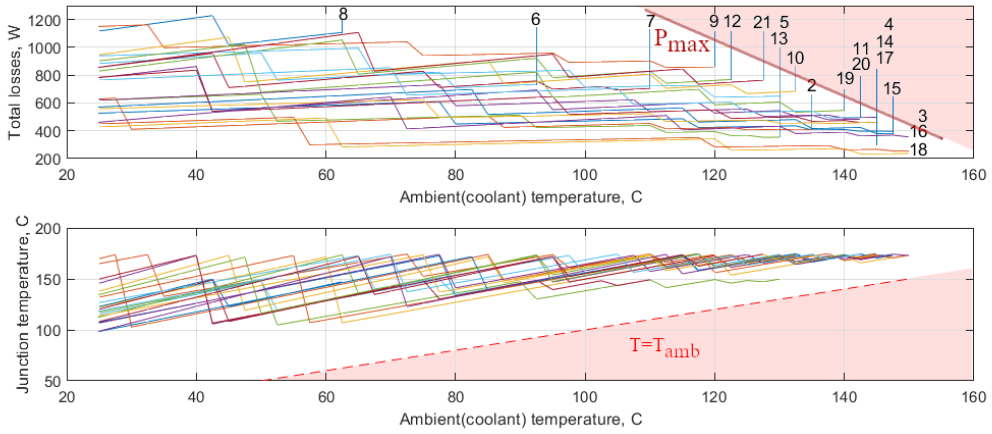


Figure 60 - Total losses and junction temperature of SMT MOSFETs in Scenario 1 (P_{MAX} represents the maximum heat that could be removed by area of 8 packages)

THT MOSFETs show excellent thermal performance as all devices can work within a specified temperature range (see Figure 61). A set of lines for maximum heat that can be dissipated by the cooler for each possible quantity of parallel devices are presented there (red dash lines), and there is some margin between actual losses and the heat value for the maximum number of parallel devices N_{PPG}=5. Therefore, those devices can operate at the ambient temperature even higher than 150°C. Another advantage of THT devices is that some have $T_{J\ MAX}$=200°C while some SMT devices are limited by 150°C.

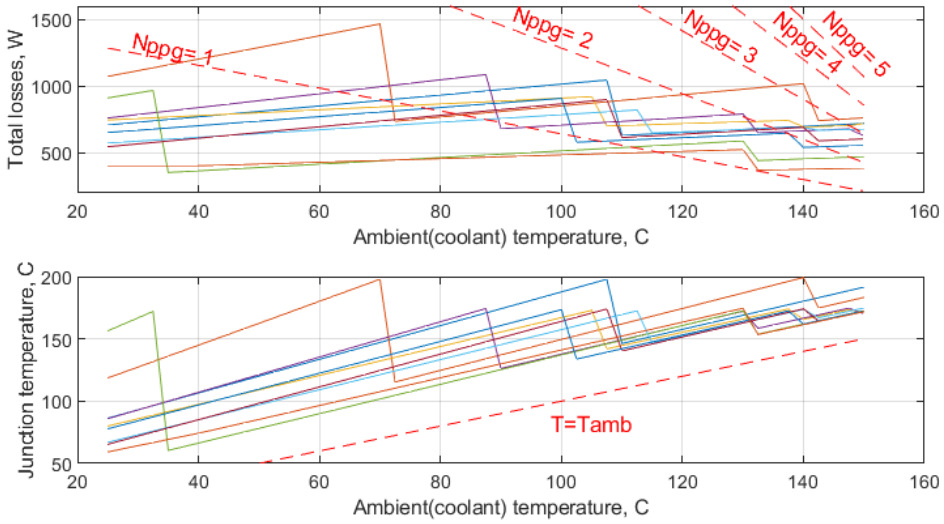


Figure 61 - Total losses and junction temperature of THT MOSFETs in Scenario 1 (red lines represent the maximum heat that could be removed by area of mentioned number of MOSFET packages)

Analysis results for power modules are shown in Figure 62, and 8 of them can operate with coolant temperature more than 105°C. However, the situation is different for power modules due to restrictions on maximum case (baseplate) temperature, which is set at 125°C for most devices. For those modules, the maximum acceptable ambient temperature should always be less than 125°C, and it is a significant drawback for HT applications.

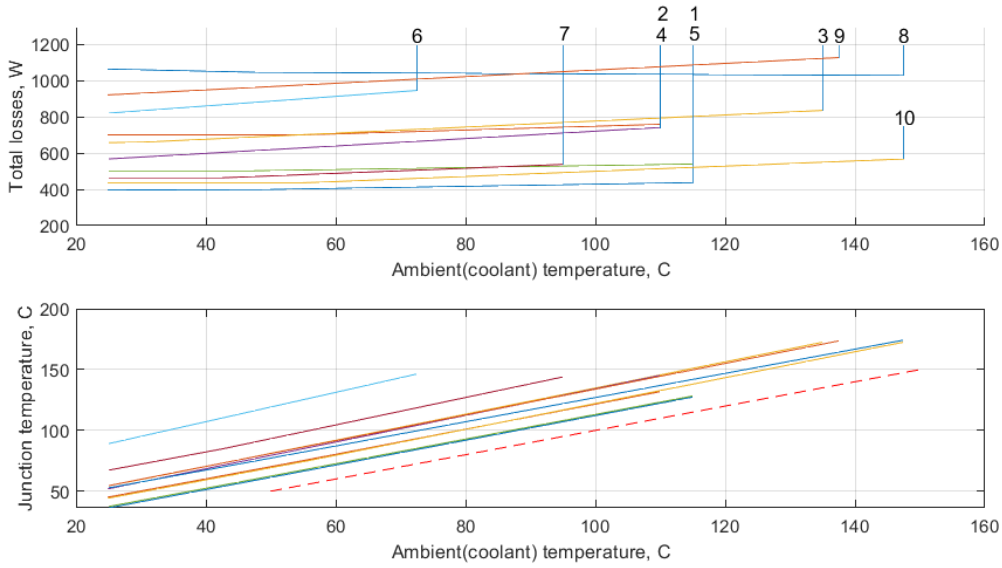


Figure 62 - Total losses and junction temperature of power modules in Scenario 1 (T_{AMB}=25÷150°C)

Conclusion on results of Scenario 1:

- If compared to power modules, discrete MOSFETs show the same average level of power losses, and THT devices also have the same junction temperature values.

- In low-power applications, discrete MOSFETs can show higher values for power densities and provide higher flexibility in power scaling and MOSFET variety. At the same time, 3-phase power modules demonstrate comparable figures in dimensional characteristics, so they also could be an excellent choice.
- All types of packages are suitable for HT applications (T_{AMB}<105°C). Unfortunately, 3-phase power modules cannot operate at such a high temperature due to great difference between junction and ambient temperature.
- THT devices show better results for T_{AMB}>105°C thanks to low junction-case thermal resistance that helps to maintain a low difference between junction and ambient temperatures. SMT devices experience difficulties transferring heat from the junction at temperatures T_{AMB}>125°C and cannot compensate for it by adding more devices in parallel. In addition, they are limited by the amount of heat that can be withdrawn by a cooling system through the area of a switching group (more efficient cooling or a large baseplate area is required). Power modules can operate under T_{AMB}>125°C, but some types are limited by maximum case temperature at T_{AMB}>115-120°C

Scenario 2. A 3-phase inverter with maximum possible values for phase current I_{Phase} and maximum DC-link voltage V_{DC} (30% safe margin for overshooting).

Target: compare inverter's maximum output power for different packages at normal and high ambient temperatures.

All devices operate at the absolute maximum of their junction temperature T_J and the maximum number of parallel devices (for discrete MOSFETs), as in this mode, the maximum output power can be achieved. In real applications, it is impractical to operate at the absolute maximum of junction temperature because of the high risks of thermal damage if any unexpected technological factors (variation in thermal resistances, grease/prepreg thickness, fluctuation of the cold plate temperature, etc.) affect heat transfer process. However, this approach can still highlight general trends, reveals issues, and helps to compare the performance of different devices in various operating conditions.

It is essential to mention that DC-link voltage V_{DC} is different for different types and equal to $0.7 \cdot V_{DC\,MAX}$; therefore, higher maximum blocking voltage helps to reach top figures in output power having average output current. Also, high output current does not guarantee the highest output power. For example, in Figure 63 SMT MOSFET №16 can handle almost 800A the highest value among SMT devices, but the output power does not

show such outstanding figures. DC-link voltage V_{DC} used in the analysis is provided in Maximum Phase Current plot above MOSFETs' bars.

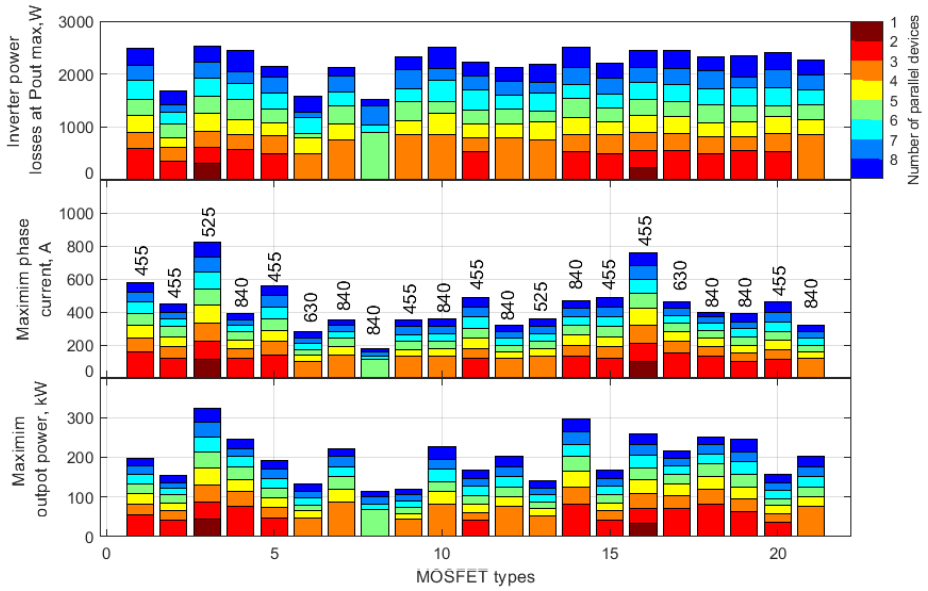


Figure 63 – Simulation results of SMT MOSFET with maximum output power T_{AMB}=25°C

Results of performance analysis under the normal ambient temperature of SMT discrete devices are presented in Figure 63 and include plots for inverter's total losses, maximum phase current (initial phase current is 100A) and maximum output power. Different colour patterns also present correlations between these parameters and the number of parallel devices. According to the results, 13 out of 21 devices reach 200kW output power, and two can provide up to 300kW. As expected, devices with 600V blocking voltage show a higher maximum phase current than 1200V devices. Although new SMT packages (PowerFLAT 8x8 HV №2 and H−PSOF8L №15) cannot deliver high output power, they can commutate decent output phase current and, therefore, be useful in height-limited applications (package height is 0.8mm and 2.3 respectfully against 4.5mm for TO-263-7).

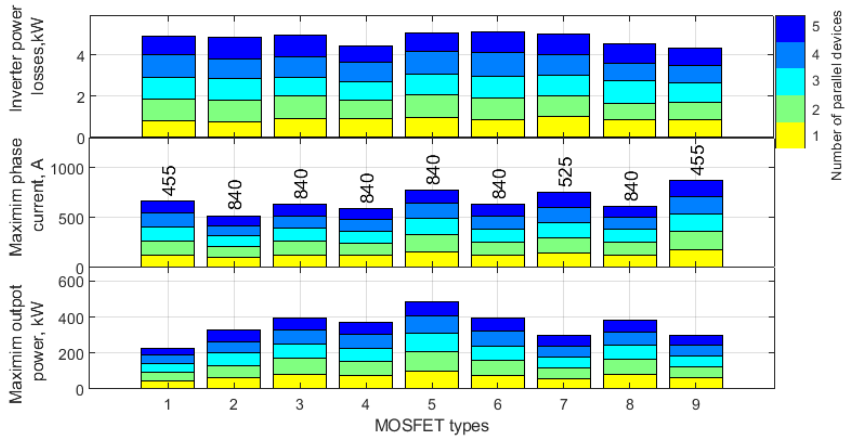


Figure 64 – Simulation results of THT MOSFET with maximum output power T_{AMB}=25°C

Results of THT MOSFETs simulation are in Figure 64 with the same set of data, and the devices demonstrate significantly higher output power (400kW and more) and an increase in total losses (more than 4kW in average) with fewer devices in parallel. This package has trends similar to SMT MOSFET ones, i.e., higher current of 600V devices with the dominant role of 1200V in maximum output power, etc.

Power module results are presented differently due to the absence of parallel connections (see Figure 65). There are graphs of $T_J(P_{OUT})$ and $P_{LOSSES}(P_{OUT})$ for each power module with the indication of DC link voltage (again, $0.7V_{DS\,MAX}$). While V_{DS} is fixed at a certain level, phase current determines inverter's output power independently from characteristics of switching devices. The maximum phase current can be obtained with the value of maximum output power and $I_{\mathrm{PH}\,MAX}(P_{OUT})$ characteristics that are presented for both DC link voltages (455V and 840V).

Due to significant deviation in characteristics, power modules show a wide range in both phase current and maximum output power. While 3-phase modules traditionally have the lowest output power, most modules can deliver 200-250kW. At the same time, the most advanced models can achieve 400-450kW with 840V of Vdc.

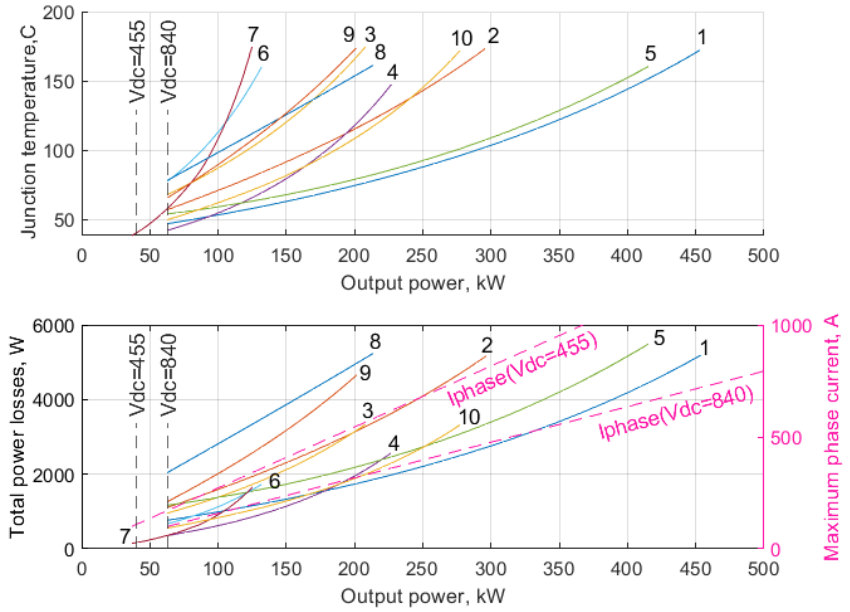


Figure 65 - Simulation results of power modules with maximum output power T_{AMB}=25°C

Results of simulations for different packages are combined in Figure 66 to facilitate a comparison of the data on the same scale. Shaded areas indicate the range of values for specific parameters for each package type, and colourful lines represent the values of three devices from each package group. SMT devices cannot compete with power modules and THT MOSFETs as they show twice less output power due to the lower blocking voltage of most powerful SMT types. Inverter's power losses follow the distribution of output power with maximum values for power modules and THT MOSFETs. At the same time, the maximum phase current is almost the same for all packages; therefore, all packages might be used in applications with limited DC link voltage (< 450V) and high phase current. Due to the maximal number of parallel devices used, the dimensional characteristics of SMT and THT devices are constant for all types (to get more details see Figure 49) and do not have shaded areas.

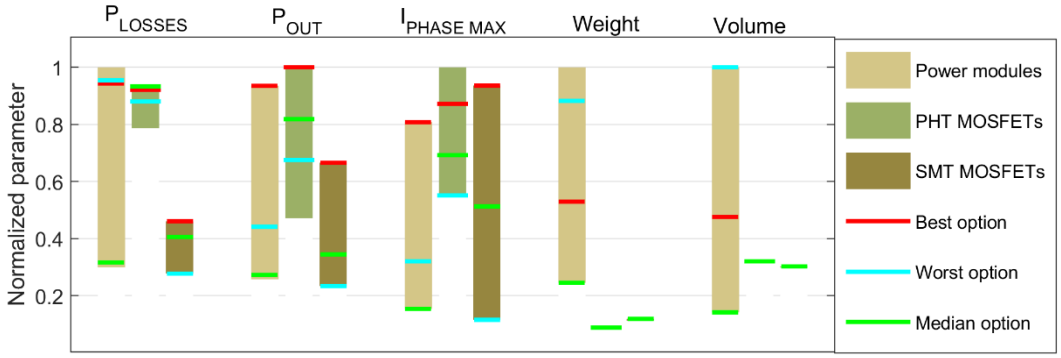


Figure 66 - Normalized analysis results for Scenario 2 conditions with T_{AMB}=25°C

Operation under high ambient (coolant) temperature T_{AMB}=105°C

Under HT operating conditions SMT devices deliver about 100kW (against 200kW at T_{AMB} =25℃) of output power on average (see Figure 67) with the maximum value of 200kW (MOSFET №3). It is also noticeable that older models (№6-8) show worse results or even cannot operate with minimum phase current. The general picture of the plots and top positions are similar to results at T_{AMB} =25℃.

HT also affects the performance of THT devices by reducing maximum output power and current (Figure 68), but all listed MOSFETs can operate with minimum required current.

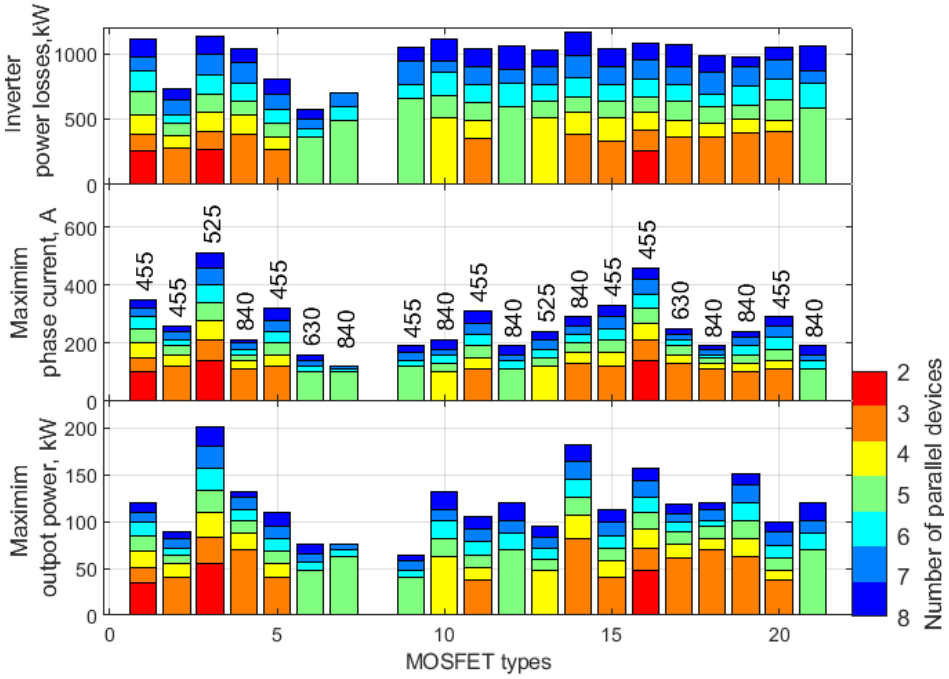


Figure 67 - Simulation results of SMT MOSFET with maximum output power T_{AMB}=105℃

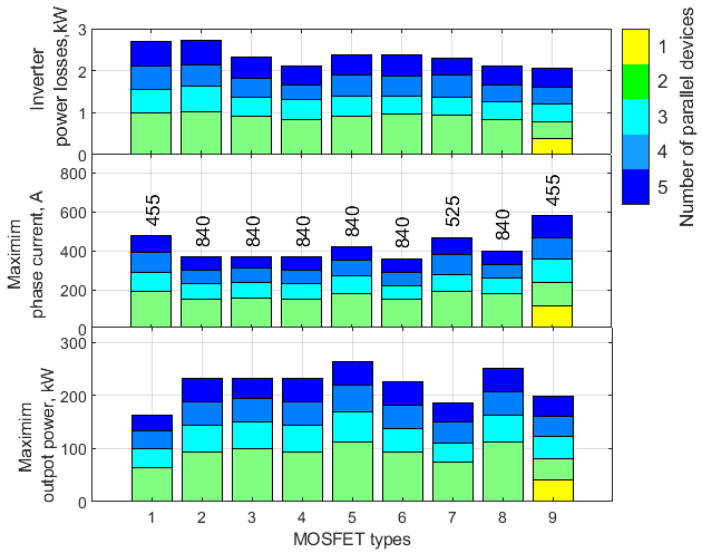


Figure 68- Simulation results of THT MOSFET with maximum output power T_{AMB}=105℃

By contrast, power modules perform much worse under HT conditions as their maximum output power is about 100kW on average (see Figure 69), comparable with SMT's results. Moreover, not all of them can operate with even minimum phase current (№2, 5, 6). The major reason for such poor performance is restrictions on case temperature, which triggers faster with higher ambient temperature. Power modules without case temperature restrictions show better results, for example, GE12047CCA3 (№10). This module, similar to discrete elements, is limited only by junction temperature, giving more freedom for temperature distribution between junction and case points. Moreover, it has a small negative coefficient $dE_{SW}(dT_J)$ that keeps its switching losses almost at the same level within a whole range of operating temperature.

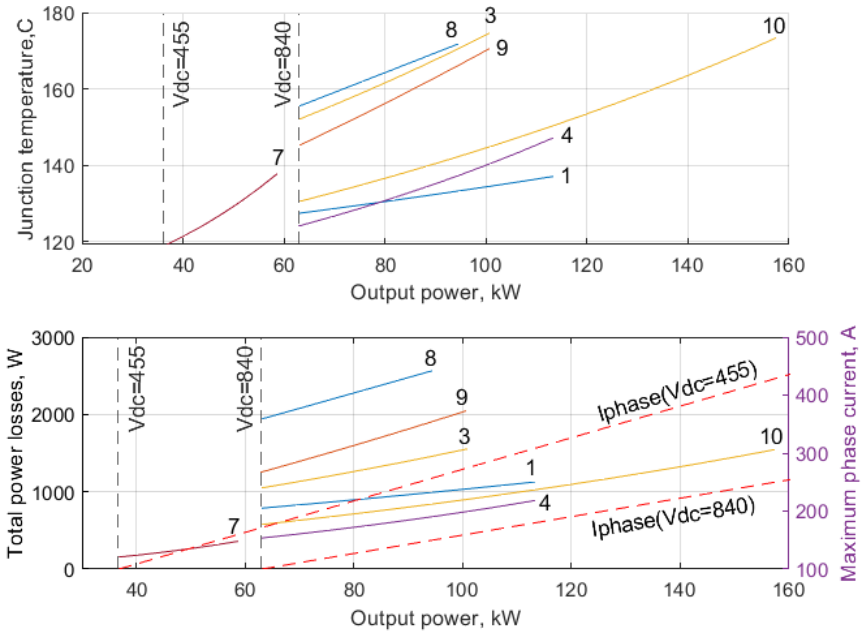


Figure 69 - Simulation results of power modules with maximum output power T_{AMB}=105°C

Figure 70 contains normalized combined data of all packages at T_{AMB}=105°C, and the dominance of THT MOSFETs is evident there. They have the highest figures in output power, phase current, and, consequently, power losses. Although SMT MOSFETs can provide less phase current with a significant reduction of power losses, only two types of SMT MOSFETs have more than 400A in maximum phase current, while most devices can handle not more than 300A. Nevertheless, SMT devices might be useful in applications with low DC voltage and high currents.

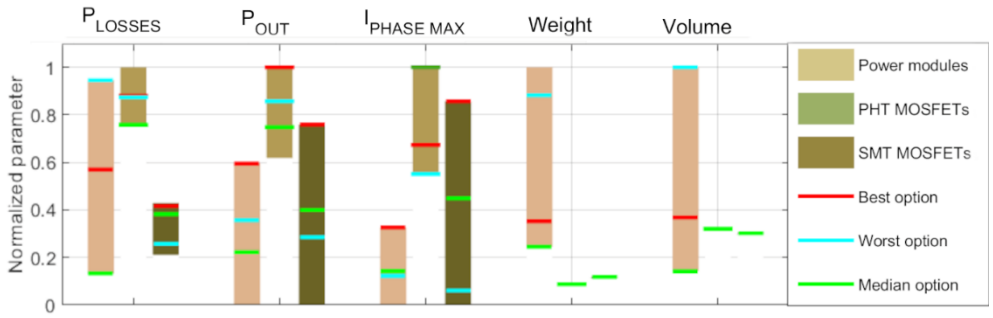


Figure 70 - Normalized analysis results for Scenario 2 conditions with T_{AMB}=105°C

Conclusion on results of Scenario 2:

- If the maximum output power is a prime target and coolant (ambient) temperature is relatively low, both power modules and THT MOSFETs demonstrate comparable performance. SMT MOSFETs achieve lower output power as their blocking voltage is lower.
- In applications with low DC voltage (<400V) some recently developed SMT

MOSFETs could operate with high phase current similar to THT MOSFETs and power modules. Moreover, SMT devices can do it in the whole range of ambient temperatures.

- All types of packages are suitable for HT applications (T_{AMB}<105℃). At the same time, the advantage of THT devices is more obvious in Scenario 2. If technological issues are not counted, this package promise to be the most flexible and effective in power scaling and thermal management.
- Requirements on maximum case temperature significantly limit power modules in HT operations, so modules that are less efficient at normal temperature might show better performance at higher temperature. This makes power modules less attractive for HT applications. In practice, however, designers, who decide to use SMT or THT devices without case temperature restrictions, might face troubles with thermal management of connectors, traces and other supplementary materials similar to those limiting power modules' case temperature.

3.4 Paralleling of SiC MOSFETs

Parallel connection of discrete MOSFET provides a significant advantage in using these types of packages due to the ability of power scaling. However, there is also a list of issues that can drastically affect the final figures and inverter's rating; therefore, they should be considered or assessed during the design process.

A) Unequal current sharing due to difference in $R_{DS\,ON}$

Different drain-source channel resistance $R_{DS\,ON}$ of parallel MOSFETs leads to disbalance in current sharing and, thus, the difference in conduction losses. If phase RMS current is considered constant, the current through a single device I_D is in inverse proportion to the channel resistance $R_{DS\,ON}$ of this device. In this example altering resistance $R_{DS\,ON2}$ of only one device (the total number of parallel devices is N) changes its value with respect to the average channel resistance of the MOSFET type $R_{DS\,ON1}$:

$$R_{DS\,ON2} = kR_{DS\,ON1}, \qquad k = 0.8 \dots 2 \tag{24}$$

Other MOSFETs of the switching group have constant $R_{DS\,ON}$ which is equal to the average value. Usually, the maximum and the average values of $R_{DS\,ON}$ are stated in MOSFET's datasheet, and the typical ratio between them ranges from 1.3 to 2. Although there is no

minimum value in datasheets, the value can be less than nominal, so the region $0.8 < k < 1$ also participates in the analysis.

Individual RMS current and conduction losses can be expressed through group current and channel resistances as follow:

$$I_{RMS\,1}\,R_{DS\,ON1} = I_{RMS\,2}\,R_{DS\,ON2}\,, I_{RMS\,GROUP} = I_{RMS\,1}\,(N-1) + I_{RMS\,2} \tag{25}$$

$$I_{RMS\,2} = \frac{I_{RMS\,GROUP}}{(N-1)k+1}\,, I_{RMS\,1} = \frac{kI_{RMS\,GROUP}}{k(N-1)+1} \tag{26}$$

$$E_{COND\,2} = I_{RMS\,2}^2 k R_{DS\,ON1}\,, E_{COND\,1} = I_{RMS\,1}^2 R_{DS\,ON1} \tag{27}$$

Results of calculations for the case $I_{RMS\,GROUP} = 100A$, N=2, 5, 10, and $R_{DS\,ON1}$=20 mOhms are presented in Figure 71.

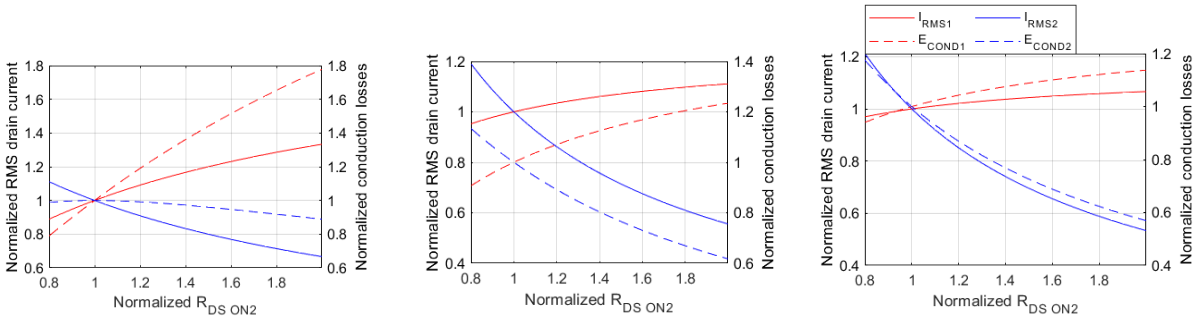


Figure 71 – Difference in drain current and conduction losses due to disbalance of $R_{DS\,ON}$ for 2, 5, and 8 parallel devices.

The most destructive effect of resistance disbalance could be observed in groups with a low number of parallel devices (N=2, 3). In the worst case of k=2 conductive power losses of MOSFET with nominal $R_{DS\,ON}$ increase by 80%. With higher N, the rise of conduction losses in MOSFETs with nominal resistance is not so rapid because the excessive current is redistributed among other devices. However, losses of MOSFET with altering resistance increase faster if $k < 1$ as the MOSFET conducts more current than others.

Positive temperature coefficient of channel resistance of SiC MOSFETs (if T_J>50-70°C) creates negative feedback for junction temperature when conduction losses of the device become higher due to lower $R_{DS\,ON}$ (device conducts more current than other devices of the group). An increase in power losses causes the rise of junction temperature that, in turn, increases channel resistance. The mechanism's effectiveness directly depends on the value of the temperature coefficient K_{RDC_ON} (where $K_{RDC\_ON} = R_{DS\,ON}(T_{J\,max})/R_{DS\,ON\,NOM}$), and at low K_{RDC_ON} it requires an unacceptably high temperature rise to compensate significant difference in resistance (examples are presented in Figure 72). Therefore, in

many cases this compensation cannot eliminate uneven current share and difference in conduction losses. Moreover, high temperature coefficient increases conduction losses in applications with high operating temperature.

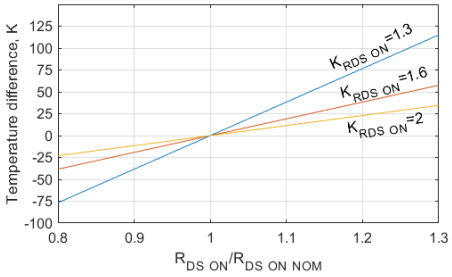


Figure 72 – Temperature difference required to compensate difference in $R_{DS\,ON}$ for various temperature coefficients ($K_{RDC\_ON} = R_{DS\,ON}(T_{J\,max})/R_{DS\,ON\,NOM}$)

Although some researchers propose techniques for active current balancing, it is hard to implement them under space and weight restrictions. Capabilities of self-equalization are limited in HT applications, but the need to have even loss distribution is higher; therefore, MOSFET chip selection might be a reasonable solution even in serial production.

B) *Unequal current sharing due to difference in gate threshold voltage V_{TH}*

According to MOSFET's datasheet V_{TH} can vary in a wide range (for example, 3.5V - 5.2V for IMZA120R014M1H), therefore, one of the paralleled MOSFETs can switch on earlier than others and start to conduct higher transient current than was expected. The actual ratio of extra current depends on many factors related to MOSFETs themself, operation conditions, and the PCB layout of the inverter. Simplified simulation of parallel MOSFETs' switching dynamics demonstrates transient processes of drain currents in case of significant difference in V_{TH} (turn-on process in Figure 73, turn-off process in Figure 74). According to the results, the difference in switching losses between two parallel devices can reach almost 70%.

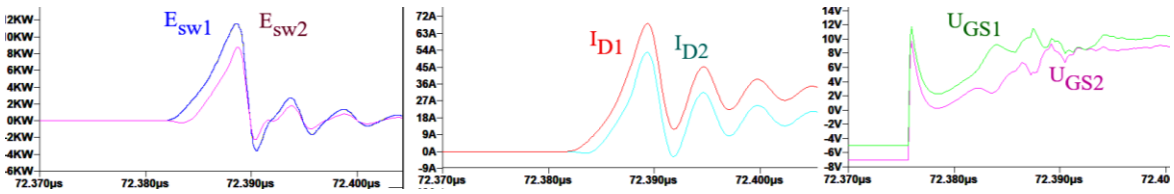


Figure 73 – Simulated turn-on of two parallel SMT MOSFET c3m0065090j with $\Delta V_{TH} = 2V$ and $\Delta E_{SW\,ON} = 42\mu J - 25\mu J = 17\mu J$

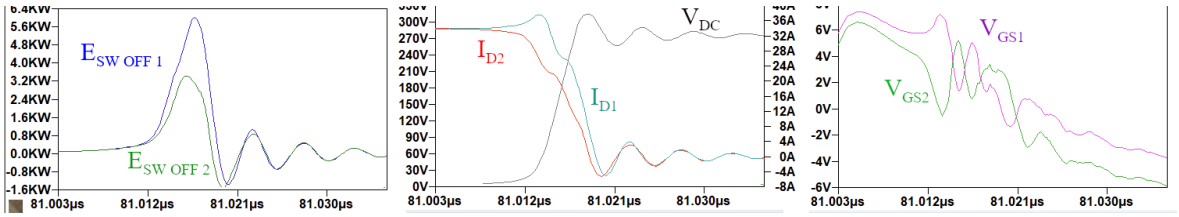


Figure 74 – Simulated turn-off of two parallel SMT MOSFET c3m0065090j with $\Delta V_{TH} = 2V$ and $\Delta E_{SW\ OFF} = 23\mu J - 13\mu J = 10\mu J$

The problem is well-studied in the literature from different points of view. For example, in [86] authors analyse deviation in MOSFET characteristics using statistical analysis to evaluate the difference in junction temperature and develop proper selection criteria. The analysis is based on measurement data from 20 samples of C2M0080120D, and power losses at switch-off vary approximately from 250 to 1100 µJ with a confidence interval of ±2σ and an expected value of 580 µJ. Another study [87] investigates the required derating of inverter's power to keep operation conditions of devices within absolute limits in case of deviation in their gate characteristics ($\Delta V_{TH} = \pm 0.7V$). The maximum difference in switching losses is stated to be below 60% and decreases with higher drain current, and the maximum value of current derating is 7%. Also authors claim that PTC of $R_{DS\ ON}$ can compensate for approximately 15% of extra switching losses by reducing the commutated current of the exact device.

The thermal model described previously does not support the difference in drain current between parallel devices, therefore it cannot predict the temperature and current distribution within a switching group. At the same time, evaluating the derating in maximum phase current is possible if the difference in switching losses is set. Current compensation caused by PTC of channel resistance is omitted to simplify analysis and because of limited effect (up to 15% of extra losses [87]). The second assumption is that heat from each device is transferred to the heatsink independently, therefore the increase of T_{CASE} of a single MOSFET does not affect the thermal conditions of others. This assumption highly relies on thermal resistance of the thermal interface and the heatsink, as high case-ambient thermal resistance increases heat transfer across the cooling surface or baseplate. As all extra losses must be dissipated through the same cooling area, either the output phase current should be reduced (output power as well) or the number of parallel devices is increased to reduce the load on each device. The results of SMT MOSFET derating are presented in Figure 75 for the case of doubling the maximum switching losses ($E_{SW} = 2E_{SW\ INIT}$),

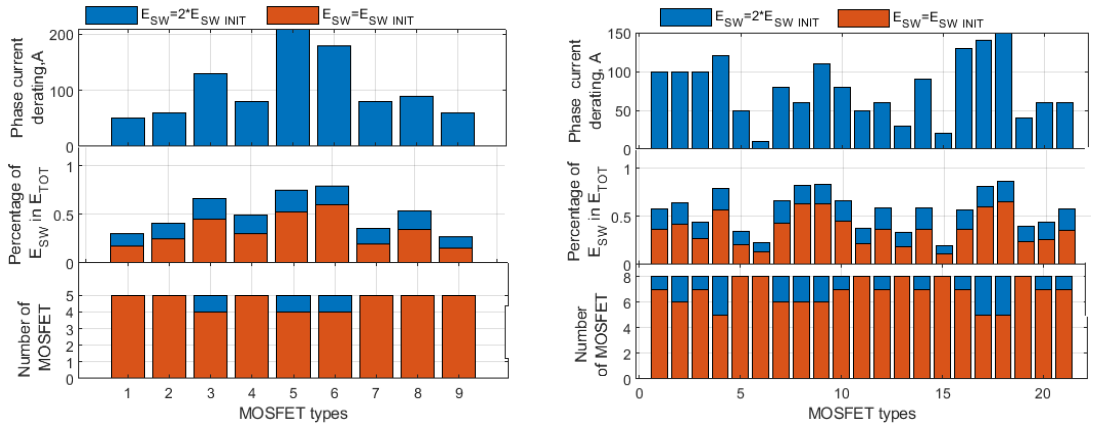


Figure 75 – Influence of doubled switching losses on THT (left) and SMT (right) devices for $T_{AMB} = 25℃$

MOSFET types which have a high percentage of switching losses experience higher derating. For SMT MOSFET, it also leads to a larger number of paralleled devices (3rd plot row in Figure 75).

Several solutions can help to reduce the detrimental effect of the problem:

- Components selection and grouping according to their characteristics. Various methods could be used to implement this technique – simple ranging by some parameter or, for example, more complicated pairing by two parameters [88]. The method is attractive due to its simplicity and absence of additional components and design modifications, but it is challenging in serial production.
- Adjustment of passive components in gate circuit. Modification of gate circuit can adjust the turn-on and turn-off behaviour of MOSFET to match the timing of other devices and decrease losses disbalance. It also requires measurements of MOSFET characteristics and sophisticated control over the manufacturing process with precision up to the exact chip. Unlike the previous method, it makes possible to use any sample of MOSFET regardless of its characteristics by changing the value of less expensive components (resistors, capacitors).
- Active balancing. The method can adjust the balance of losses with high accuracy but requires a considerable number of additional components to measure the current of each device, and hardly applicable for a large number of parallel MOSFETs.

C) Other reasons for unbalanced parallel MOSFET operation:

- *Not optimal PCB layout*. Imperfections in layout design, such as unequal trace length, non-symmetrical component locations[89], trace cut, serial connection of power and signal lines[90] etc., can lead to disbalance in current sharing. An

accurate and precise investigation is required in each case to develop a proper solution as layout issues are highly individual. The incorrect layout can affect the MOSFET performance by gate signal disturbance leading to gate signal oscillations or fluctuations in the edges of gate signal (the effect is similar to variation in threshold voltage). Also, layout might affect current sharing by introducing uneven parasitic inductances of drain/source traces for different MOSFETs in the same group. In this case, transient drain currents also become unbalanced despite the simultaneous gate dynamics.

- *Heating by neighbour MOSFETs and uneven cooling with complex PCB shape*. The assumption is made in the thermal model that temperature spreads evenly across the baseplate or surface of the heatsink. In reality, the central part of the baseplate or heat sink area beneath the MOSFET group has a higher temperature than the border region. In the case in Figure 76 the temperature difference between central and edge MOSFETs is approximately (69°C-64°C)/(69°C-20°C)≈10%.

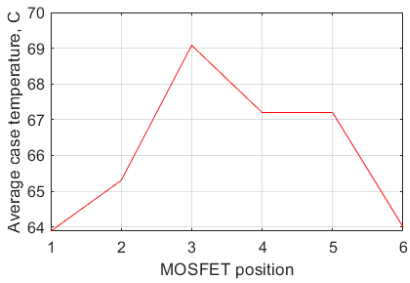


Figure 76 – Measured average case temperature of 6 MOSFETs connected in parallel (package TO-220 attached to IMS and water cooling, P_{MOSFET}=15W)

In addition, the complex shape of the baseplate/heatsink can include extra side regions that cool MOSFETs closest to the border of the switching group. FEA usually is required to obtain an accurate picture of temperature distribution

3.5 Effect of advanced thermal conductive materials and cooling techniques.

Further improvement of inverter's performance could be achieved by adopting of advanced thermal conducting materials and cooling methods. Ceramic heat spreader or ceramic PCB, as it was mentioned before, provides different pattern of heat distribution along and through the cooling structure by comparison with IMS. As ceramic has equal thermal conductivity in both directions, it does not need to be as large as IMS to utilize the heat conducting area with the same efficiency.

Performance analysis of inverters with ceramic PCB and enhance cooling shows significant improvement with new conducting material (Kcer=25W/mK is typical for high grade material, plate thickness 1mm), but limited effect of the modified cooling. Initial heat transfer coefficient is 0.5W/cm^{2}K which is typical for pipe cooling method, and the improved version has 1W/cm^{2}K what is average value for pin fin water structure or single phase microchannel cold plate. Average total thermal resistances of a MOSFET (does not include its inner resistance) for 3 cases (IMS, ceramic, improved cooling) are 2.53, 2.2, 1.5 respectively. In Figure 77 results of simulation are demonstrated. It is noticeable that increase in output power for case with ceramic PCB does not match the rise of power losses, normalized losses ($100\% * \frac{P_{LOSSES}}{P_{OUT}}$) are higher in average by 17% because higher MOSFET current causes non-linear change of channel resistance and switching losses.

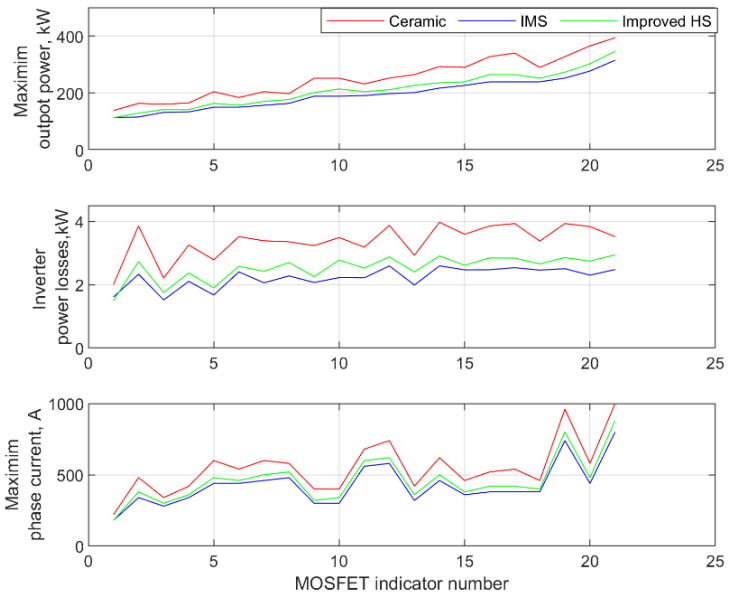


Figure 77 – Effect of ceramic PCB and improved cooling on performance of inverter with SMT MOSFETs.

3.6 Comparison of 2-level and 3-level inverters

A) Modifications in analysis's methodology:

A number of modifications in the calculation method are added to utilize it with 3-level inverters:

- Unlike the simple 2-level topology, many 3-level inverters are featured by uneven power loss distribution between their switching groups. Different switching groups might have different switching frequencies and RMS currents. Moreover, various MOSFET combinations might be more efficient than a homogenous set of MOSFETs introducing additional requirements to the inverter's model. The modified calculation model has to consider individual losses and junction temperature for each group by using its specific coefficients to obtain accurate results.
- A modulator is introduced inside the model calculate switching losses based on the number of switching events and instant values of MOSFET voltage and current. The previous model uses a simplified equation which is not applicable for multilevel topologies and advanced modulation methods of 2-level inverters. An ordinary SPWM with 2 level-shifted carriers is used for NPC and TNPC, and LF-HF SPWM is used for ANPC, however, they can be replaced with more complex modulations if necessary.
- Conduction and switching loss patterns for MOSFETs and diodes are described manually in the model for each topology according to the direction of phase current and the value of modulation voltage.

B) Input arguments and combinations for analysis:

The initial arguments for the analysis are specified in Table 16. The overall analysis is similar to the analysis of scenario #2 from chapter 3.4. The output parameters for analysis are total losses, maximum achievable phase current and maximum output power of an inverter.

The results indicate performance at the maximum number of parallel MOSFETs per group with a limit of 16 per phase if it is not specified in the description. In most cases, a 2-level inverter has 8 parallel devices in each switching group, TNPC has 4 devices per group. ANPC inverter has 6 switching groups per phase, therefore this inverter uses different numbers of devices per group (T1,4 – 3 pcs, T2,3 – 3 pcs, T5,6 – 2 pcs) to

maintain the total number of 16 devices per phase. NPC inverter has 4 switching group and 2 groups of diodes per phase, so each switching group has 3 MOSFETs, and each diode group has 2 parallel diodes.

Table 16 – Initial conditions for performance analysis

Parameter	2-level	3-level		
		NPC	TNPC	ANPC
Number of MOSFETs per phase	16 (2x8)	16 (2x3+2diodes)x2	16 (2x4)x2	16 (3+3+2)x2
Maximum phase current, A	20÷800, step 20A			
Maximum DC link voltage, V	0.7 $V_{DC\ MAX}$	0.7 $2V_{DC\ MAX}$	0.7 $V_{DC\ MAX}$	0.7 $2V_{DC\ MAX}$
F_{SW}=50 kHz, F_{FUND}=1250 Hz, φ=20º, M=0.95, T_{AMB}=25°C				

Table 17 – Variations in topologies for performance analysis

Stage	Combination	Topologies for comparison	Comments
1a	Same MOSFET types in all groups	2-level, 3-level	
1b		2-level, 3-level+lower F_{SW}	F_{SW}=25 kHz for 3-level F_{SW}=50 kHz for 2-level
2	Different MOSFETs	TNPC+HV MOSFET(T2, T3)	HV MOSFET type is #18
3	Different number of MOSFETs in groups	ANPC+Reduced N_{PPG} of LF	$N_{PPG\ T1} = 2$, $N_{PPG\ T2} = 3$, $N_{PPG\ T5} = 1$

In Figure 78 results of analysis are presented with 5 plots for different parameters, and they are sorted by the maximum output power of 2-level configuration so that the highest figures are at the right side (position does not match the number in Table 9). Comparison of unmodified inverters (stage 1a, Table 17) shows the following:

- 2-level inverter, in general, offers higher possible output power than other topologies due to the highest phase current. At the same time, its efficiency shows the worst figures, therefore, total power losses are also the highest in the analysis.
- NPC and ANPC topologies can operate with higher DC voltage, but the maximum phase current is lower than 2-level and TNPC can conduct. Total power losses are also the lowest among the topologies considered. ANPC performs better than NPC because of lower conduction losses (MOSFET vs diode) and the absence of switching losses for some groups.
- TNPC topology reaches the highest phase current among considered 3-level topologies, which might be useful in high current but low voltage applications

with strict requirements on THD of output current.

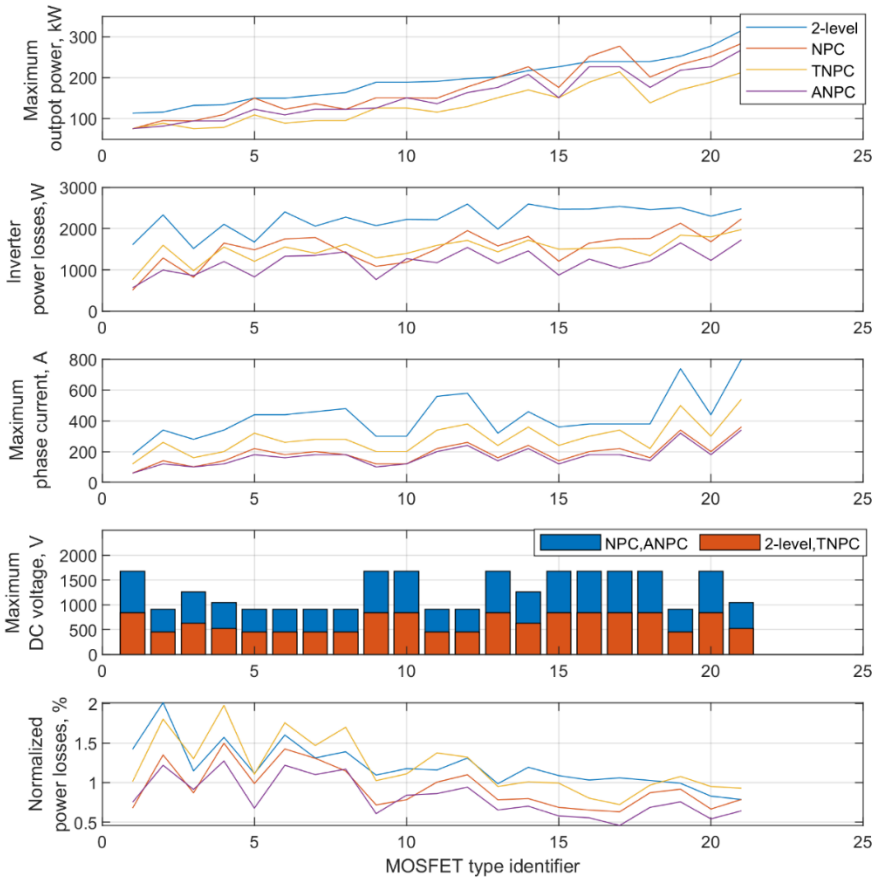


Figure 78 – Comparison between 2-level and 3-level topologies (MOSFET type identifier is different from previous chapters)

Additional levels in the shape of phase voltage reduce current ripples and THD. So multilevel converters could work with lower switching frequency maintaining the same level of current ripples or distortion. In stage 1b 3-level inverters work with twice lower F_{SW} that, in theory, should reduces switching losses and increases $P_{OUT\ MAX}$. In Table 18 results are presented in the shape of $P_{OUT\ MAX}$ normalized by $P_{OUT\ MAX\ 2-LVL}$ for each topology.

Table 18 – Effect of reduced switching frequency on the inverter's performance

Switching frequency	Average $P_{OUT\ MAX}$ normalized by $P_{OUT\ MAX\ 2-LVL}$								
	NPC			TNPC			ANPC		
	Total	HV*	LV	Total	HV	LV	Total	HV	LV
F_{SW}=50 kHz	0.87	0.88	0.85	0.68	0.7	0.65	0.79	0.8	0.77
F_{SW}=25 kHz	0.92	0.96	0.88	0.71	0.74	0.67	0.86	0.89	0.82
	+0.5	+0.8	+0.3	+0.3	+0.4	+0.2	+0.7	+0.9	+0.5

HV – cases with V_{DC}>600V

Results show significant difference in the effectiveness of switching frequency reduction for high (V_{DS}>800V) and low voltage (V_{DS}<800V) devices. All types demonstrate higher achievable power with a lower frequency, but devices with high drain voltage more affected by the switching frequency due to higher portion of switching losses in total

power dissipation. Devices with lower V_{DS} have to conduct higher drain current to provide the same output power, and their conduction losses dominate in total losses generated by MOSFET, so the effect of lower switching losses does not lead to noticeable improvement.

More levels give additional flexibility in adjusting of inverter's characteristics by applying different types of MOSFETs for different switching groups. For example, the maximum V_{DC} of TNPC topology is determined by V_{DS} of T1, T4 and by $2V_{DS}$ of T2, T3. Therefore, V_{DC} could be increased if T1 and T4 are high-voltage MOSFET, or conduction losses of T2, T3 could be reduced if MOSFETs with lower V_{DS} are used there. In Figure 79 simulation results of the performance analysis for such modifications are presented. Modified inverters have the same maximum DC link voltage of 840V as other unmodified HV TNPC inverters. Type of MOSFET for the substitution is selected individually for each case to match the performance of initial MOSFET and do not provide advantage due to high performance of only one switching group.

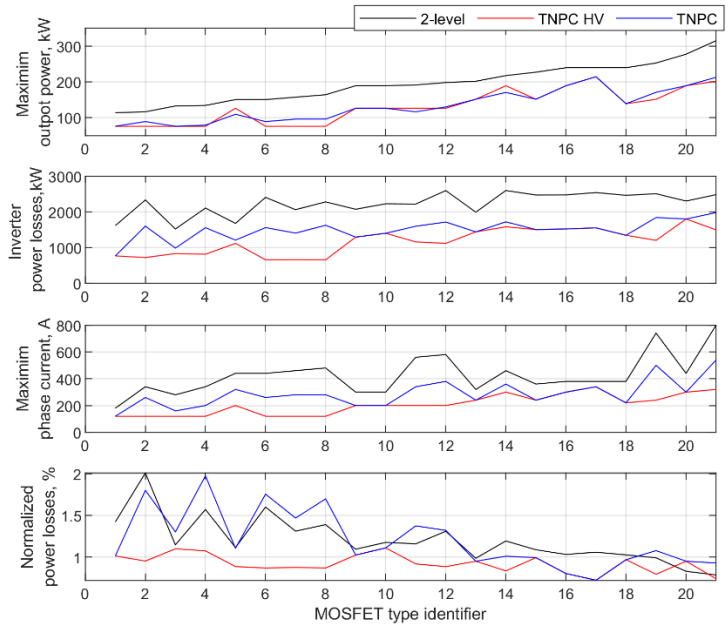


Figure 79 – Simulation results of modified TNPC topology

Modified versions experience a small drop in maximum output power, conduct significantly lower phase current, and have lower losses as well (see Table 19). Efficiency of new inverters is slightly higher than efficiency of HV inverters made out of only one MOSFET type (see Table 20).

Table 19 – Change in performance of TNPC after MOSFET substitution.

Inverter	Avg. $\frac{I_{PH}}{I_{PH\ 2LVL}}$	Avg. $\frac{P_{LOSS}}{P_{OUT}}$, %	Avg. $\frac{P_{OUT}}{P_{OUT2LVL}}$
No modification*	0.65	1.4	0.65
HV MOSFETs applied	0.37(-43%)	0.9(-36%)	0.62(-5%)

* - only for MOSFETs V_{DS}<600V

Table 20 – Comparison between homogeneous and modified HV TNPC

Inverter	Avg. P_{LOSS}/P_{OUT}, %			
	<76kW	76kW÷140kW	140kW÷170kW	180kW<
Homogeneous HV TNPC	1.01	1.04	0.97	0.83
Modified HV version	0.96	0.9	0.8	0.8

By contrast with the 2-level topology, switching groups of 3-level inverter could differ not only by MOSFET type but also by the number of devices in a group. Due to different proportion of conducting current in different operating modes (combination of φ and M) the number of MOSFETs per group might be adjusted to optimize the total number of MOSFETs and, thus, the dimensions of the inverter. In stage 3 of the analysis smaller number of devices is used in ANPC topology (12 instead of 16) to demonstrate advantages and limitations of such approach.

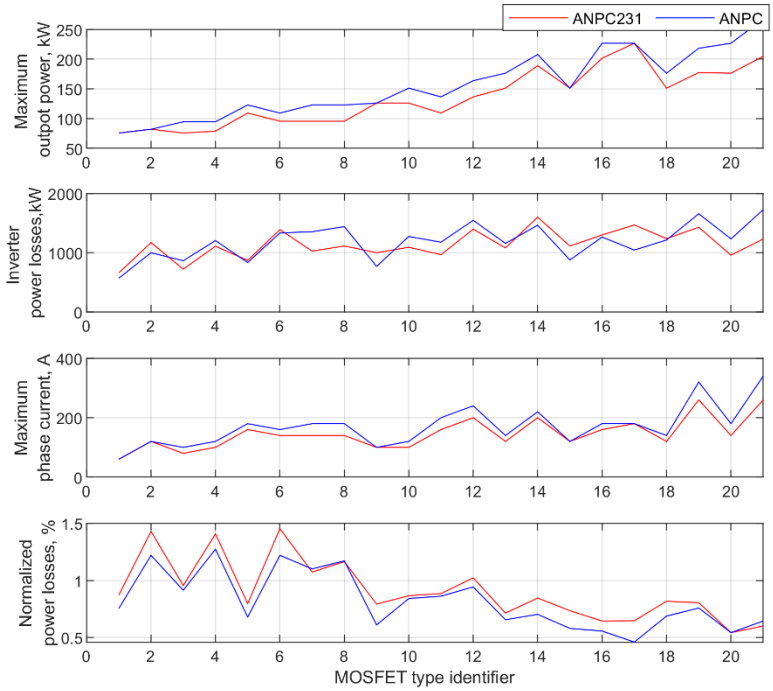


Figure 80 – Performance of ANPC topology with 25% reduction of MOSFET quantity.

Although the number of MOSFETs is smaller by 25%, reduction in the maximum output power is vary from 0 to 23% (see Figure 80). At the same time, efficiency declines for many MOSFET types, and power losses per device jump significantly increasing demand

for effective cooling and reducing overall reliability.

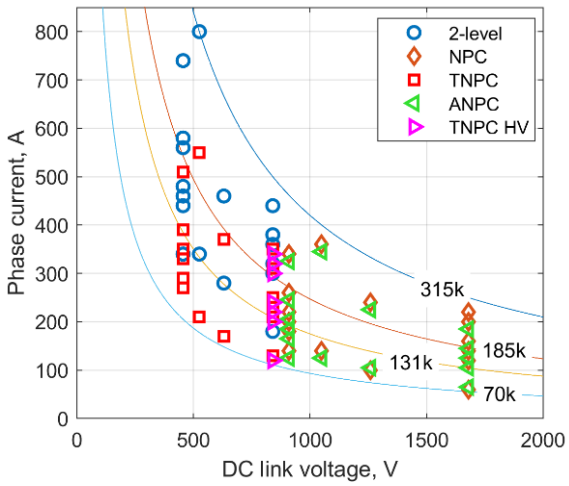


Figure 81 – Summary diagram of performance comparison between 2- and 3-level inverter topologies (lines and figures indicate levels of inverter output power).

Analysis results are summarised in Figure 81 indicating areas with the best utilization of each topology. Although area of application might be shifted to lower DC voltage with some increase in phase current, output power will decrease.

Summary:

- For the specified number of MOSFETs 2-level inverters demonstrate higher output power, higher phase current, higher power losses, and lower efficiency in the most cases.
- 3-level topologies might be helpful if the reduced THD or high efficiency are required. High DC-link voltage is also important factor to consider multilevel topology as more MOSFET types are available for the application. At the same time, higher number of switching groups might cause rise in the volume of supplementary and control electronics as well as sophisticates the control algorithms.

3.7 Power density analysis for integrated motor drive system.

A) Methodology of IMD dimensional analysis:

Integration of an inverter and a motor, as mentioned in Chapter 2, aims for the maximum power density and often dictates the shape and dimensions of the inverter to increase utilization of inner space or area. The design of the drive is complex from the mechanical point of view compared to non-integrated variants because several systems (cooling, mechanical, electrical etc.) should be located close to each other or even share the same space and operate without difficulties. The simulation model of the inverter that also considers the mechanical characteristics of the integrated machine could be developed to evaluate possible values for power density. Machine mechanical design and system structure partially determine the inverter's location and additional requirements for the PE shape. For example, a central opening is often required in EAEp design for shaft extension, an encoder, or bearings.

Relationships between different parts of design model are presented in Figure 83 The machine design stage is the first in system development and can be performed as soon as the preliminary system characteristics (DC voltage, output power, maximum dimensions etc.) are finalized. The machine model is not presented in this research, and it acts as a black box with a list of input and output parameters (only inverter-related parameters are mentioned):

- **Electrical parameters**

  Input: Output power P_{OUT}, switching frequency F_{SW}, phase voltage V_{PH}, fundamental frequency F_{FUND};

  Output: Phase current $I_{\mathrm{PH}\ MAX}$, power factor η;

- **Thermal parameters**

  Input: Ambient temperature T_{AMB}, coolant temperature $T_{COOLANT}$, coolant flowrate Q_{COOL} and pressure P_{COOL}; *No Output parameters*

- **Mechanical parameters**

  No Input; Output parameters: weight W_{IMD}, dimensions $L \times \mathrm{W} \times \mathrm{H}$, housing outline (border shape, opening, cooling inlet etc.)

The thermal model of the inverter uses the amplitude of phase current from the machine's design. Power factor is omitted in the flowchart as its effect is insignificant with PMSM, but it could be added easily in analysis to increase accuracy. In real applications,

the results of the machine's mechanical design determine the inverter's outline in some individual way, but in this study, such interactions are simplified. Therefore, only the round and square PCB shapes represent the possible limitations introduced by the machine. Machine's requirements for thermal characteristics of coolant (flowrate, pressure, etc.) are also omitted, though too small flowrate or significant pressure drop in PE heatsink might affect thermal conditions of the machine in real applications. Electrical and mechanical parameters important for calculations are presented in Figure 82

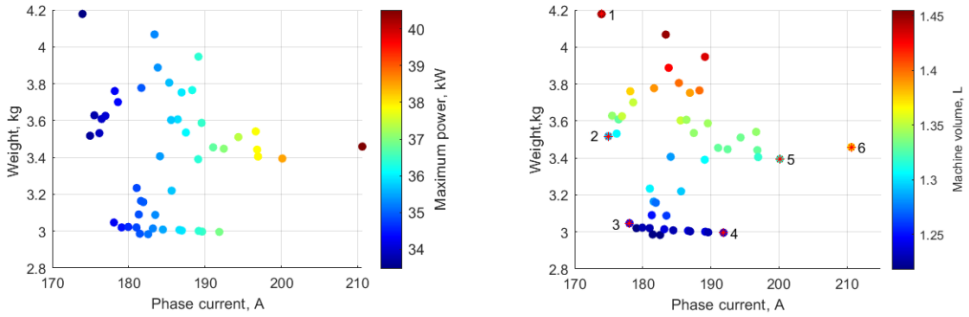


Figure 82 – Relation between machine's mass and phase current of motors used.

In Figure 82 (right plot), the numbers next to markers show motors that are selected for further analysis due to extremum values of their characteristics (for example, lowest phase current, highest power etc.). Although the target power P_{OUT} is 30kW, and some machines do not operate at their maximum power, it would be interesting to observe the effect on inverter characteristics.

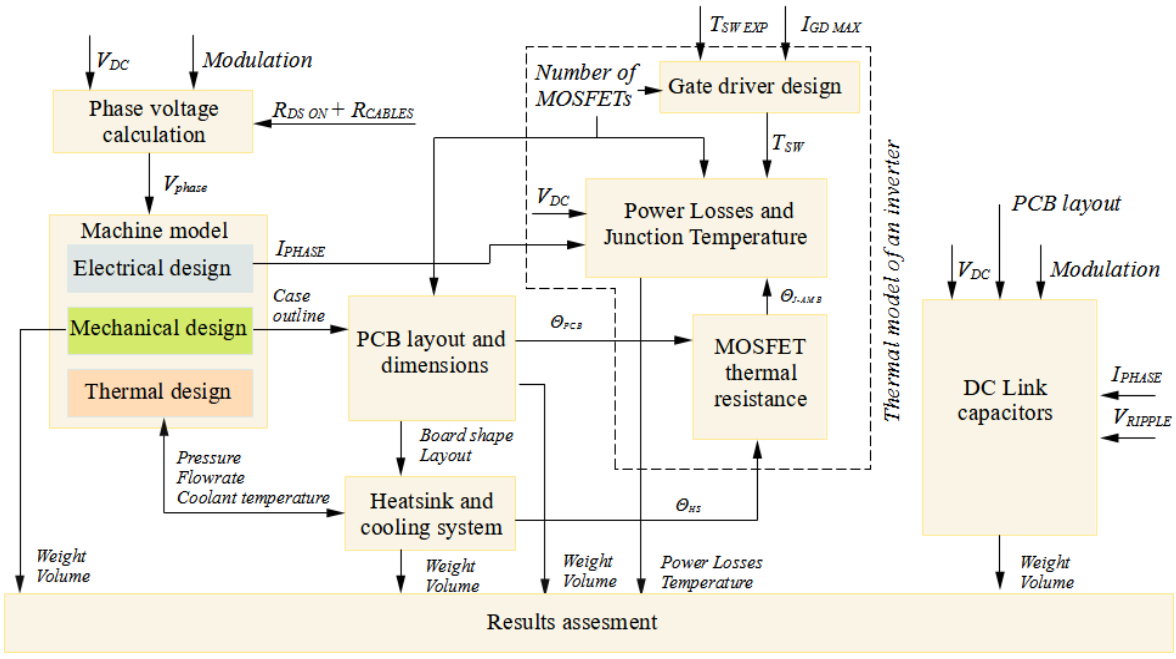


Figure 83 – Flowchart of IMD combined calculation model

Thermal characteristics of the PCB (for SMT devices) and the heatsink are also required to start inverter design; therefore, initial materials involved in heat transfer and the heatsink type should be selected in advance. The operation of the thermal model is similar to the one described above, and the heat transfer coefficient of the heatsink is not constant anymore. The coefficient depends on PCB geometry and size for some cooling types (for example, with water channel), and the number of paralleled MOSFETs affects initial values.

The proposed model works for SMT components only, but the same method is applicable to simulate inverters with THT MOSFETs or power modules after some modifications.

B) PCB layout estimation and calculation of cooling performance

According to the literature review and analysis of commercially produced prototypes (see Figure 17), the most popular inverter shapes are round (with or without a central hole) and rectangular. Modular inverters and multiphase inverters also could be divided into several PCBs, but the board structure is significantly different in this case, so they are out of our consideration here.

Simplified examples of rectangular and round PCBs and a prototype of a round PCB are presented in Figure 84.

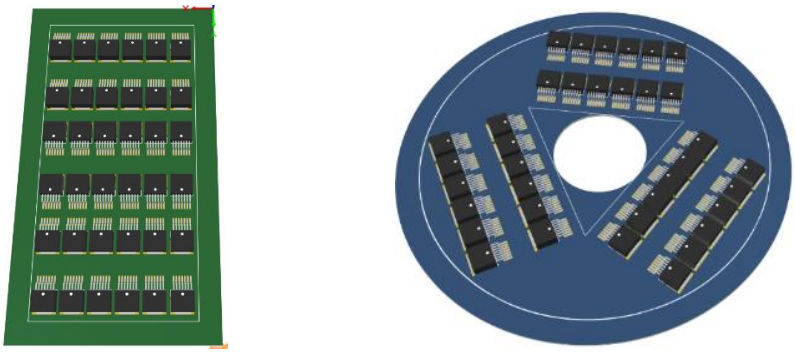


Figure 84 – Two different shapes of PE PCB.

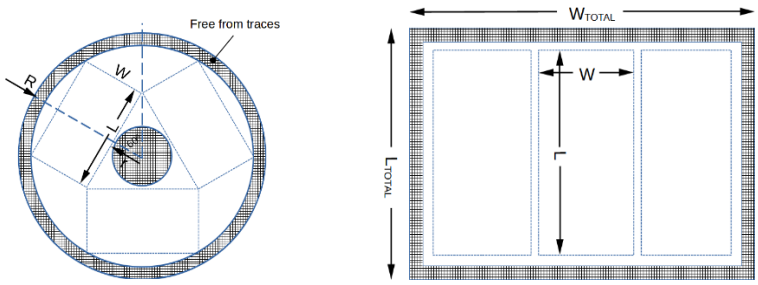


Figure 85 – Layout structure of round (left) and rectangular (right) PCB

Dimensions of PCB that can accommodate the required number of MOSFET are

expressed through the dimensions of the switching group (see Figure 85):

$$R = \sqrt{\left(\frac{L}{2\sin(60°)} + W * \cos(60°)\right)^2 + (W * \sin(60°))^2} + (10 \div 15)mm \quad (28)$$

$$r = \frac{L}{2\tan(60°)},\ S_{ROUND} = \pi(R^2 - r^2)$$

$$L_{TOTAL} = \mathrm{L} + 2 \cdot (10 \div 15)mm, \qquad W_{TOTAL} = 3\mathrm{W} + 2 \cdot (10 \div 15)mm$$

$$S_{RECT} = L_{TOTAL} W_{TOTAL}$$

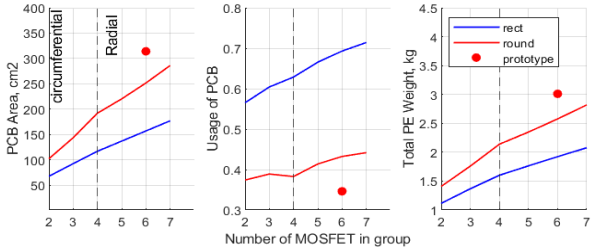


Figure 86 - Comparison of round and rectangular PCB shapes for different number of transistors in a group.

The rectangular layout is featured with the better utilization of PCB surface, as it has a smaller area (see Figure 86). Therefore, it shows better figures for the weight of power electronics, so that layout should be considered first if mass restrictions are applied. However, integration with a machine sometimes requires a more complex design of power electronics when the rectangular shape does not satisfy the requirements. In that case, the proposed round design could be the only option. At low value of N_{trans} the round layout is more efficient with circumferential orientation of switching groups rather than with radial as the length of the group becomes smaller than its width.

Prototype PCB also has a round shape due to the needs of the machine's structure. Additionally, the diameter of the prototype PCB has been increased to have more freedom for design and assembling, but strict space optimization of connections and auxiliary circuits can achieve theoretical values shown in Figure 86.

C) Water cooling and cold plate design

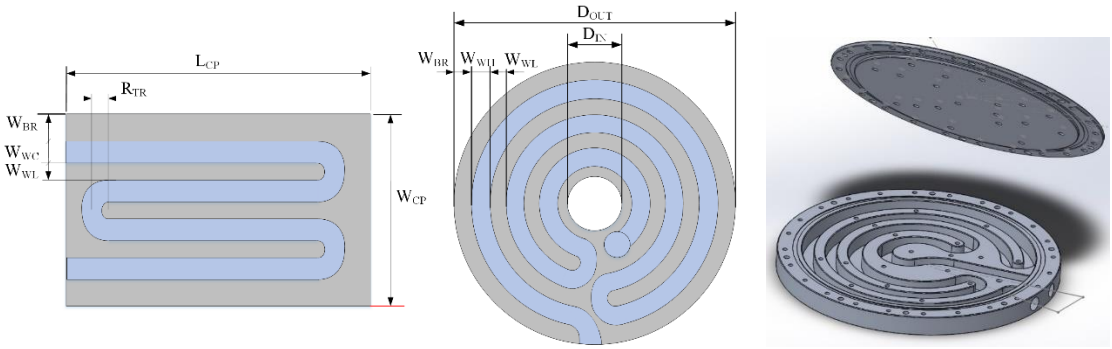


Figure 87 – Structure of water channels for different PCB shapes.

The analysis includes two types of cold plate structures (with milled water channels and fin areas). Despite the complex distribution of water channels across the cold plate, the assumption is made that its thermal resistance is considered uniform and equal to the average at any point of a cold plate. Channels occupy as much area of a cold plate as possible.

Total thermal resistance depends on the length of the water channel, its section and water flow rate. As the dimensions of the power board are different for different N_{PPG} it is necessary to determine maximum length of channel (L_{ch}), i.e., maximum number of passes across the cold plate (N_{pass}). Structure characteristics such as wall thickness W_{WL}, border margin W_{BR}, inner hole diameter D_{IN}, channel dimensions W_{CH} are highly individual and determined by system, manufacture, and technical requirements. Values used in the analysis are mentioned in Table 21 and demonstrated in Figure 87.

Table 21 – Parameters of the water channel

Parameter	Value
Wall thickness W_{WL}, mm	3
Border margin W_{BR}, mm	5
Channel dimensions T_{CH}, W_{CH}, mm, mm	5/10
Inner hole diameter D_{IN}, mm	20
Min turn radius R_{TR}, mm (if pipe is used)	10

Assuming that heat exchange happens only by means of water cooling, inverter total power losses are equal to the rise of coolant temperature (ΔT) times coolant specific heat and its mass:

$$P_{inv} = \Delta T C_{P\ Liq} \rho_{Liq} F_{Liq}, \tag{29}$$

where P_{inv} – total inverter losses, $C_{P\ Liq}$ is coolant specific heat, ρ_{Liq} is coolant density, and F_{Liq} is flow rate. At the same time, heat conducted through the cold plate follows Newton's law:

$$P_{inv} = h_{Liq} L_{CH} A_{CH} \left(T_{CP} - T_{IN} - \frac{\Delta T}{2} \right), \tag{30}$$

where h_{Liq} is heat transfer coefficient, L_{CH} is length of water channel, A_{CH} is its perimeter, T_{CP} is temperature of the cold plate, and $\left(T_{IN} + \frac{\Delta T}{2} \right)$ is average coolant temperature along the channel.

Combining these equations together the hermal resistance of the cold plate could be derived as follows:

$$\theta_{HS} = \frac{1}{h_{Liq} L_{CH} A_{CH}} + \frac{1}{2 C_{P\ Liq} \rho_{Liq} F_{Liq}} \tag{31}$$

Calculation of heat transfer coefficient h_{Liq} requires calculating Reynolds number (Re),

Prandti number (Pr) and Nusselt number (Nu) according to Dittus-Boelter equation:

$$h_{Liq} = Nu\frac{K_{Liq}}{D_{hydro}}; Nu = 0.023Re^{0.8}Pr^{0.4};\ Re = \frac{F_{Liq}}{S_{WC}}D_{hydro}\frac{\rho_{Liq}}{\mu_{Liq}};\ Pr = C_{P\,Liq}\frac{\mu_{Liq}}{K_{Liq}}, \tag{32}$$

As the heat source locates on one side of the cold plate only, and wall thickness is relatively small, only part of the channel surface participates in the heat transfer (coefficient of 0.5 applied in calculations).

The length of the water channel is determined by the maximum number of channel passages across the radius (for round shape) or one of the sides (for rectangular shape):

$$N_{turns} = \begin{cases} \left\lfloor \frac{D_{out} - D_{in} - 2W_{BR} + 2W_{WL}}{2(W_{WL} + W_{CH})} \right\rfloor, for\ round\ shape \\ \left\lfloor \frac{W_{CP} - 2W_{BR} + W_{WL}}{W_{WL} + W_{CH}} \right\rfloor, for\ rectangular\ shape \end{cases} \tag{33}$$

$$L_{CH} = \begin{cases} \pi N_{turns}(D_{in} + W_{CH}) + 2\pi \sum_{k=1}^{N_{turns}} (k-1)(W_{WL} + W_{CH}), for\ round\ shape \\ 2(W_{BR} + W_{CH}) + N_{turns}\left(L_{CP} - 2(W_{BR} + W_{CH})\right) + \cdots \\ \frac{\pi}{2}(N_{turns} - 1)(W_{CH} + W_{WL}), for\ rectangular\ shape \end{cases} \tag{34}$$

Results of calculation are presented in Figure 88. Although round shaped cold plate shows lower total thermal resistance due to a larger surface, the normalized resistance of the MOSFET group is lower for the rectangular shape.

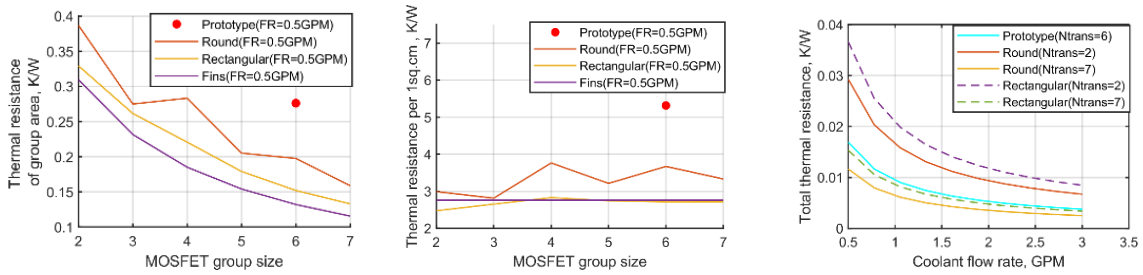


Figure 88 – Characteristics of a cold plate with different Ntrans, layout, flow rate and cooling techniques.

The cold plate with fins requires complex theoretical analysis to obtain its thermal resistance formula; thus, a commercial off-shelf cold plate CP30 (manufactured by ASM) was used for the comparison. The prototype's normalized figures are lower than theoretical due to the larger area of PCB. Because of integration with a machine, the maximum dimensions of the surface accommodating water channel are limited.

The total volume of IMD includes machine and inverter volumes that are calculated according to schemes in Figure 89:

$$\mathcal{V}_{INV} = \begin{cases} \pi(\mathcal{T}_{COLDPLATE} + H_{MOSFETs} + H_{PE1} + \mathcal{T}_{WALL})(\mathcal{T}_{WALL} + R_{PCB})^2 + 0.5L \\ (\mathcal{T}_{COLDPLATE} + H_{MOSFETs} + H_{PE1} + \mathcal{T}_{WALL})(\mathcal{T}_{WALL} + L_{PCB})(\mathcal{T}_{WALL} + W_{PCB}) + 0.5L \end{cases}, \tag{35}$$

$$\mathcal{V}_{EM} = \pi(L_{EW} + L_{ACTIVE} + L_{SEW} + \mathcal{T}_{FP})\left(\mathcal{T}_{WALL} + \frac{OD_S}{2}\right)^2,$$

where $\mathcal{T}_{COLDPLATE}$=15mm, H_{PE1} – height of supplementary PE part (H_{PE1}=50mm), $\mathcal{T}_{WALL}$=3mm, L_{EW}=10mm, L_{SEW}=45mm, $\mathcal{T}_{FP}$=10mm. The values are obtained from reference design of 30kW IMD with reasonable margins for manufacturing, maintenance etc. Nevertheless, they might vary due to individual optimization and requirements. Values of $H_{MOSFETs}$, R_{PCB}, L_{PCB}, W_{PCB}, OD_S, L_{ACTIVE} are subject to machine and MOSFET characteristics.

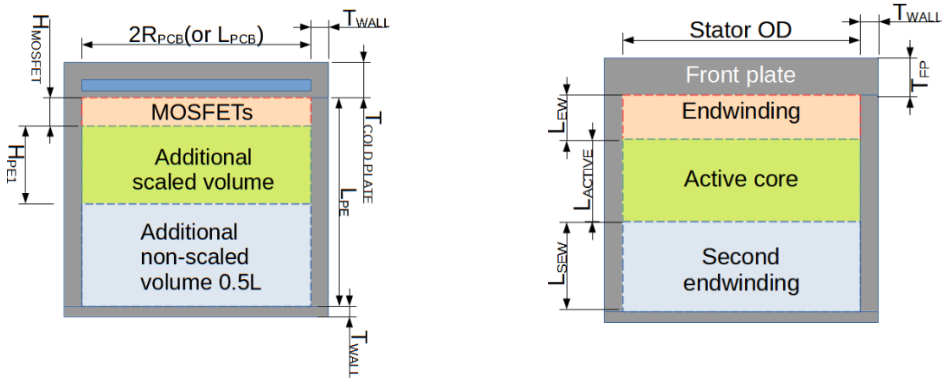


Figure 89 – Scheme for inverter (left) and machine (right) volume calculation.

The machine's weight is the output of the machine calculation model, and that value is used in the IMD model to calculate the total weight. The PE's weight includes mainly the mass of housing and an additional non-scaled value of 1 kg to represent elements of mechanical structure, PCB, sensors, etc.

Results of density estimations for all possible variants of machine and numbers of parallel MOSFETs are shown in Figure 90. As expected round shaped PCB has lower values due to the larger area. It is noticeable that EM is responsible mainly for the gravimetric power density of the IMD. Although inverter size has a limited effect on total IMD weight, the contribution of the PE part can reach almost half of the total value at a large number of parallel devices. By contrast, PE influence on volumetric power density is significant (almost 50-75%) due to less dense content. Also, figures of some prototypes and commercial IMD are presented in Figure 91 for comparison.

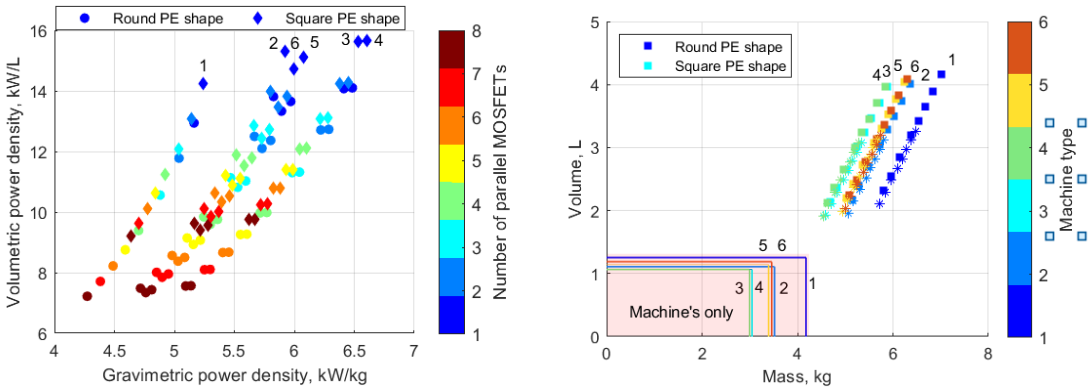


Figure 90 – Possible values for power density with different machines (right) and number of parallel devices (left)

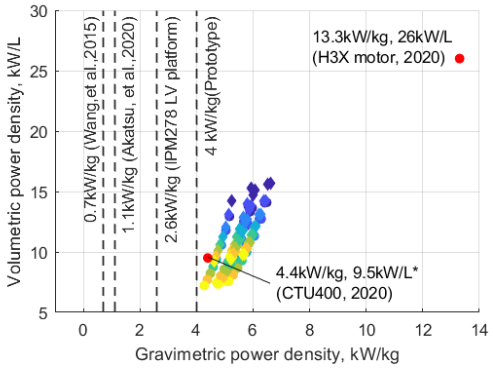


Figure 91 – Comparison with characteristics of other IMDs.

Results of thermal model simulation at $T_{AMB} = 105℃$ and $T_{AMB} = 25℃$ are presented in Figure 92. As expected, power densities are lower at a higher ambient temperature, but the difference is insignificant (less than 10%). High temperatures limit the maximum densities by 6.3kW/kg and 13 kW/L.

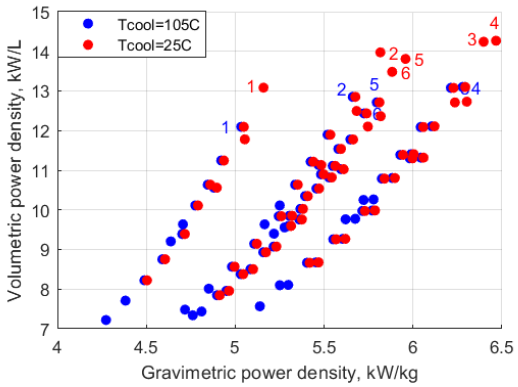


Figure 92 – Power densities of IMDs at $T_{AMB} = 105℃$ (blue) and $T_{AMB} = 25℃$ (red).

The difference in junction temperature between pipe and fin technologies is also insignificant (see Figure 93) due to the high thermal resistance of PCB and MOSFETs themselves. At the same time fin cold plate offers better distribution of coolant due to its design, therefore, possibility of hotspot is also lower.

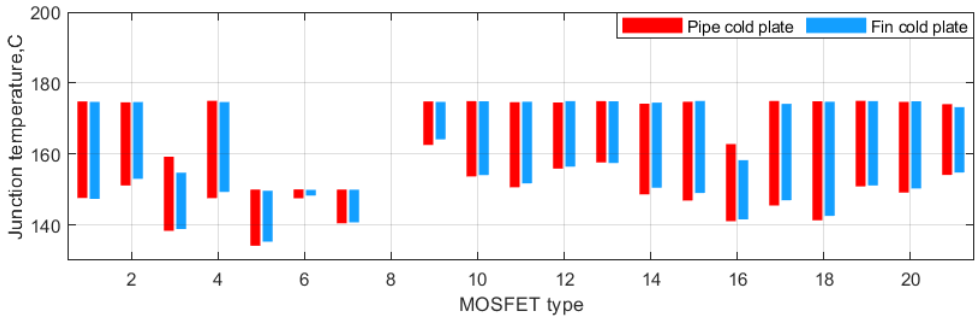


Figure 93 – Junction temperature for different MOSFETs and cooling

Additional results highlighting the relationships between inverter's total losses and power density are presented in Figure 94. The significant difference in losses for different machines happens for a low number of parallel devices and becomes smaller with adding more MOSFET in parallel due to a decrease of individual current. MOSFET type has a major influence on power losses.

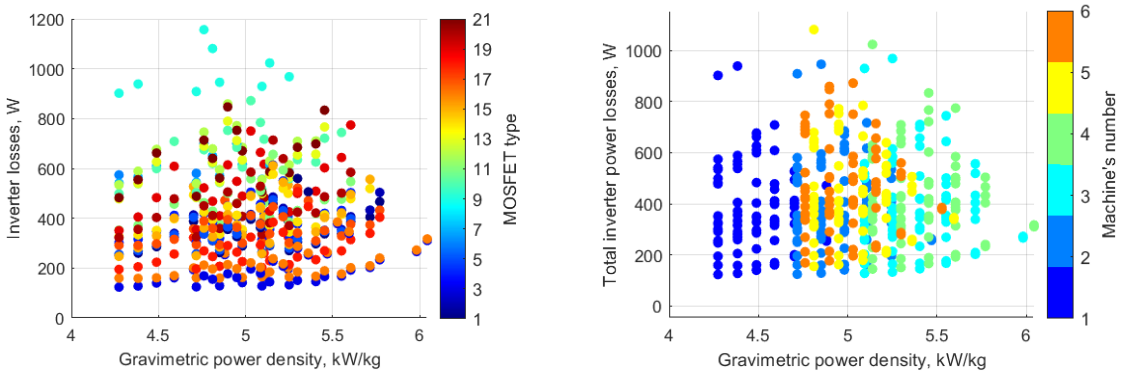


Figure 94 – Inverter power losses for different MOSFET and machine types ($T_{AMB} = 105℃$, only round PCB, only pipe cooling, only 6 machines)

Conclusion:

- The proposed model is able to evaluate various parameters of IMD and their influence on the final characteristics of IMD;
- With given characteristics of machines (PMSM, high-speed operation, etc.) PE mainly contributes to the volume of IMD occupying 50-75% of total space. Therefore, it is challenging to develop IMD with the same diameter for both machine and inverter, especially with a round shape.
- MOSFET characteristics significantly affect the performance and dimensions of the inverter. Usage of modern devices leads to lower losses, lower junction temperature, and a wider range for output power. Package unification of SMT components might play an essential role in the fast modification of the inverter to

increase load current or efficiency without PCB redesign.

- IMS PCB with typical thermal characteristics of prepreg and copper thickness (2W/mK 100μm, 2oz Cu), dense chip layout, and high value of junction-case thermal resistance diminishes the importance of the heat sink's performance. A simple pipe structure gives similar results to a modern fin structure if no hotspot is created due to uneven distribution of the channels or temperature gradient. Advanced IMS or ceramic substrate material could be used to improve overall thermal performance.

3.8 DC-link capacitor sizing.

A) Calculation of required capacitance of DC-link

The DC-link capacitor provides a short path for the inverter's AC current and eliminates the negative effect of the power source's parasitic inductance. Although DC-link capacitance does not affect the performance of power devices directly, it is essential to investigate its characteristics due to following reasons:

- High-temperature capacitors are not widely available in the market, and most of them are ceramic capacitors, therefore, it could be challenging to obtain high values for DC-link capacitance.
- Low DC-link capacitance might lead to difficulties with control stability due to high voltage ripples. Estimation for required capacitance should be done during the early stage of the development process, as it could be impossible to increase capacitance later due to volume constraints.
- Some capacitors have a bulky package and might reduce the total power density of the inverter, which is a crucial parameter for IMD.

The main electric target parameter for a DC-link capacitor is the amplitude of voltage ripples $\Delta V_{R\,PP}$ of DC-link voltage V_{DC}. Voltage ripples depend on both hardware characteristics of the inverter and the modulation strategy; therefore, a large number of factors are involved in the analysis. RMS current through the DC-link capacitor is another important parameter that has to be calculated to guarantee acceptable operating conditions for the capacitors. Too high RMS current leads to capacitors overheating and, in turn, reduction in their lifetime or damage.

The typical structure of the 2-level 3-phase inverter is presented in Figure 95. The inverter has balanced 3-phase loads with amplitude of phase current I_{PH} and sinusoidal

PWM switching pattern.

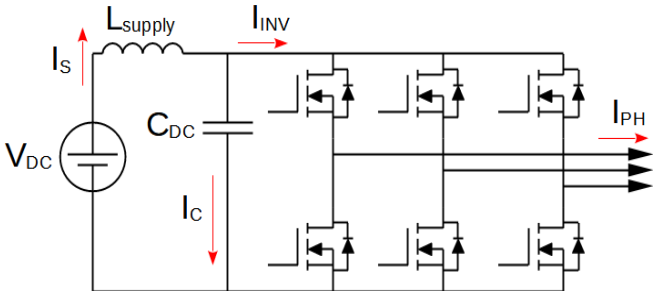


Figure 95 – Currents involved in operation of DC-link capacitor of 2 level 3 phase topology.

Active losses of wires and MOSFETs, current instability, and voltage fluctuations of V_{DC} are not included into the analysis. In this case, phase current i_{PH} and output voltage (for the first phase) could be expressed as follows:

$$i_{PH\,A} = I_{PH}\sin(\omega_F t - \varphi)\,, v_{PH\,A} = V_{PH} M \sin(\omega_F t), \tag{36}$$

where ω_F – angular fundamental frequency, M – modulation index [0;1].

Due to the nature of power supply lines a significant part of high-frequency AC current I_C flows through the DC-link capacitor while the power supply provides the inverter with direct current I_S only. This assumption becomes more accurate if the resonant frequency of the low-pass filter created by L_{SUPPLY} and C_{DC} is much lower than the switching frequency F_{SW} of the inverter[91]. By analysis of switching currents and voltage the expression for RMS current through DC-link capacitor is obtained:

$$I_{C\,RMS} = I_{PH\,RMS}\sqrt{M\left(\frac{\sqrt{3}}{2\pi} + \left(\frac{2\sqrt{3}}{\pi} - \frac{9}{8}M\right)\cos^2\varphi\right)} \tag{37}$$

In [92] further analysis is done to express equations for voltage ripples based on the current diagrams during the period of $[0; \frac{\pi}{6}]$:

$$\Delta v_{R\,PP} = \frac{I_{PH}}{C_{DC} F_{SW}} r_{PP}(M, \varphi, \omega_F t), \tag{38}$$

where

$$r_{PP} = \max\left(r_{PP1}, r_{PP2}\right), \tag{39}$$

$$r_{PP1} = \frac{3M}{8}\left(1 - \frac{\sqrt{3}}{2} M sin\left(\frac{\pi}{6} + \omega_F t\right)\right) cos\varphi,$$

$$r_{PP2} = \frac{3M}{8}\left|\left(1 - \frac{\sqrt{3}}{2} M sin\left(\frac{\pi}{6} + \omega_F t\right)\right) cos\varphi + \frac{4}{\sqrt{3}} sin\left(\frac{\pi}{6} - \omega_F t\right)\left(\frac{3}{4} M cos\varphi - cos(\omega_F t - \varphi)\right)\right|$$

Phase angle can be fixed at the value of 20-25º as only PMSM motor type with a power factor >0.9 is considered a load. Actual phase value $\omega_F t$ could be omitted if the amplitude of the ripple's envelope (i.e. maximum values of ripples in the period of $[0; \frac{\pi}{6}]$) is used in the calculation. In this case, r_{PP2} has a simple approximation function valid for the exact value of PF:

$$r_{PP}(\varphi = 20°) = 0.328M - 0.212M^2, \tag{40}$$

Results of calculation are presented in Figure 96 with a test set of characteristics to demonstrate the behaviour of the target parameters ($\Delta V_{R\,PP}$ and $I_{C\,RMS}$) under various operating conditions. The maximum of characteristics lies between 0.6 and 0.8 of the modulation index. Therefore, the system with a higher maximum speed (i.e. higher operating voltage) experiences a higher capacitor current due to a lower modulation index. A higher phase current to produce the same amount of torque also increases the difference.

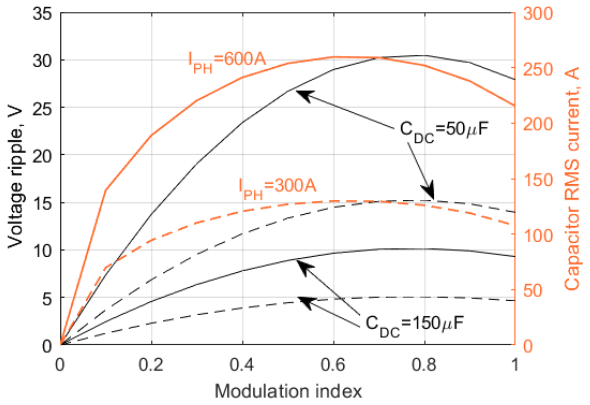


Figure 96 – Voltage ripples and capacitor RMS current for different values of modulation index, phase current (solid line – 600A, dash line – 300A) and capacitance at $F_{SW} = 50kHz$

Acceptable value of $\Delta V_{R\,PP}$ is selected according to the needs of the drive control algorithm. For most control systems it is acceptable to specify the maximum ripple level as a percentage of V_{DC} rather than have an absolute value of fluctuations. Thus, the absolute value $\Delta V_{R\,PP}$ increases with a higher V_{DC} (see Figure 97). For this analysis the value of $0.03V_{DC}$ looks like a good typical estimation for voltage ripples.

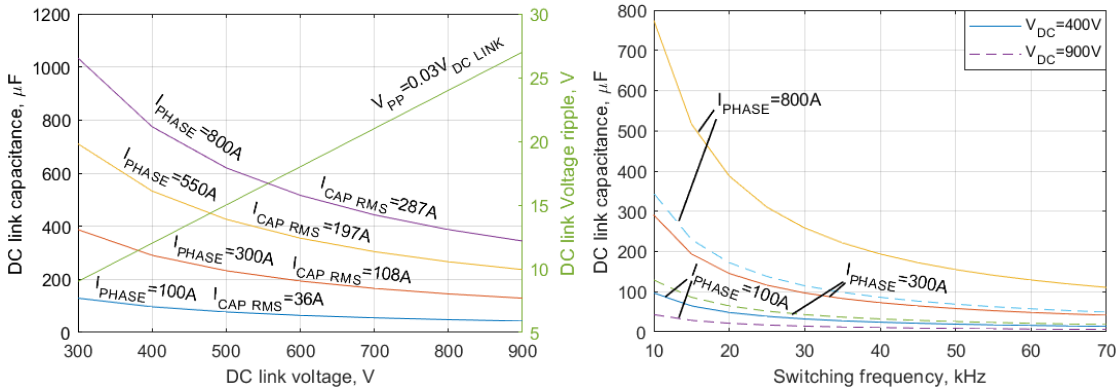


Figure 97 – Required value of DC-link capacitor to maintain specific level (3% of V_{DC}) of voltage ripples under different operating conditions (M=1)

Based on the chosen maximum $\Delta V_{R\,PP}$, required capacitance is calculated for various F_{SW}, V_{DC}, and I_{PHASE} to indicate the order of capacitance. Both increase in V_{DC} and F_{SW} leads to decrease of minimal DC-link capacitance, but at low F_{SW} the capacitance might reach such a high value that it become challenging to obtain that level without electrolytic capacitors. Graphs in Figure 97 highlight the advantages of having a higher switching frequency and DC-link voltage V_{DC}.

B) <u>High temperature and high voltage DC-link capacitors.</u>

The variety of capacitors featuring both high operating temperature and high DC voltage is even more limited than the variety of MOSFETs due to a small number of applications that demand such a combination. Nowadays, the most widespread type of HT capacitors is ceramic capacitors made of HT ceramic materials (including C0N, N1500, X7R, PLZT) that can withstand temperatures up to 200℃. HT film capacitors are also presented in the market, but the maximum temperature does not exceed 150℃, and its volumetric capacitance is much lower. Information regarding the capacitance density of HT capacitors is presented in Figure 98. PLZT capacitors show the best combination of dimensions, temperature, and capacitance. The common drawback of HT capacitors is low volumetric capacitance by comparison with low-temperature electrolytic ones. Although the maximum capacitance of a single capacitor reaches dozens of μF, its large size often makes it difficult to place them inside IMD.

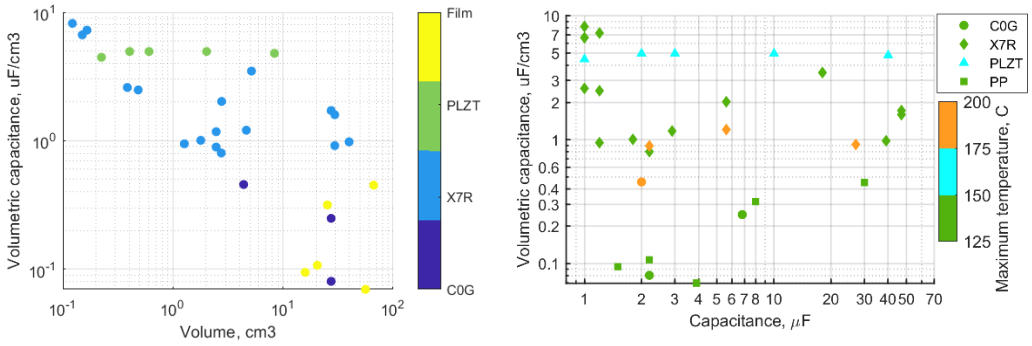


Figure 98 – Distribution of volumetric capacitance for HT HV capacitors.

More detailed data of capacitors used in further analysis is listed in Table 22.

C) Estimations of minimal quantity of capacitors under different operational conditions

The algorithm of the sizing process is presented in Figure 99. Some capacitors have derating of maximum capacitance value at high temperature or high voltage, and this feature is included in the calculation model. The maximum RMS current changes with the switching frequency for all ceramic capacitors (not valid for film capacitors in selected frequency range).

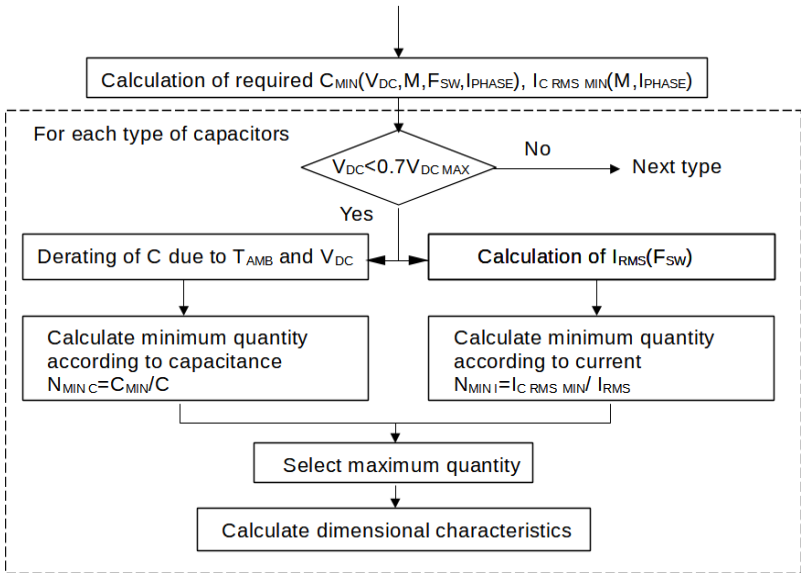


Figure 99 – Flowchart of DC-link capacitor sizing process

All current characteristics are for the ambient temperature of 105°C. The normal thermal model (through thermal resistance and dissipating power) is challenging to apply to capacitors with acceptable accuracy due to the non-linear temperature dependency of capacitance and ESR. Although temperature of 105°C is only used in the analysis, the changes in capacitance for all types of materials are shown in Figure 100. PLZT has more

complex function C(T) for lower temperature, but it is skipped here.

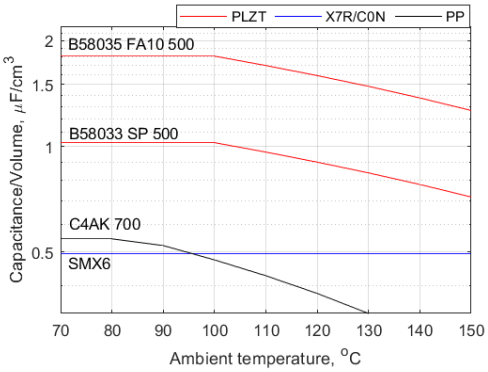


Figure 100 – Temperature related derating of capacitance for different materials

Results with values for total volume and total area (area of each capacitor is increased by 1mm on each side to account mount and leakage clearances) are demonstrated in Figure 101. Film and ceramic capacitors show different behaviour due to limitation mechanisms applied. Total DC-link capacitance determines the number of ceramic capacitors and has a negative bias with increased switching frequency. Therefore, the volume and area of ceramic capacitors decrease with the frequency. Total DC-link current limits the number of PP capacitors due to their low maximum RMS current. As a result, the number of PP capacitors does not change with the frequency. PP capacitors need a smaller value for the total area at low frequency than some of the ceramic capacitors (because of the difference in capacitors' height).

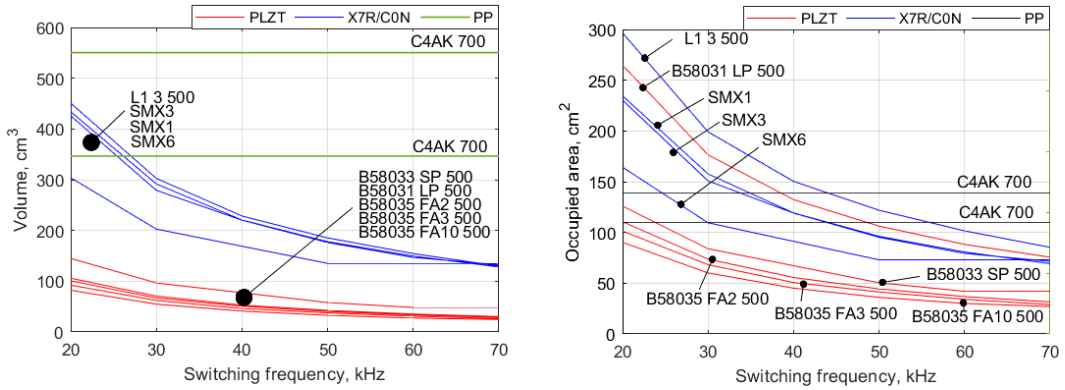


Figure 101 – Total volumes and areas of DC-link capacitor within specified range of switching frequency (M=1, V_{DC}=400V, $I_{PHASE} = 300A$).

In order to evaluate the required additional volume accommodating DC-link capacitors inside IMD, dimensions of PCBs calculated previously during the SMT MOSFET analysis are used here. The only rectangular shape is used for this calculation due to simple methods to solve “packing” problem and obtain the maximum quantity of capacitors per PCB. In Figure 102 and Figure 103 the maximum figures are presented for the total number of capacitors, maximum capacitance, and maximum RMS current. Area analysis

does not include any connections, fixing components, and other components, except the keep-out area of 10mm along the edge of the PCB. It is important to highlight that each application target limits the number of capacitors significantly and in different ways according to its own features and restrictions, and these numbers are used only to show general trends in the design of DC-link capacitor bank. Moreover, it might be economically disadvantageous to use these number of capacitors due to high prices for some components (the total price for capacitors could become higher than the price of power semiconductors) unless required by specific applications.

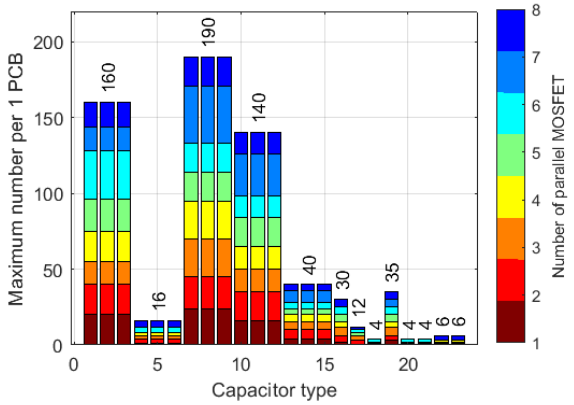


Figure 102 – Maximum quantity of capacitors per PCB

It is worth to mention that film capacitors offer the same total capacitance per a single PCB as PLZT ones, however their total RMS current is significantly lower.

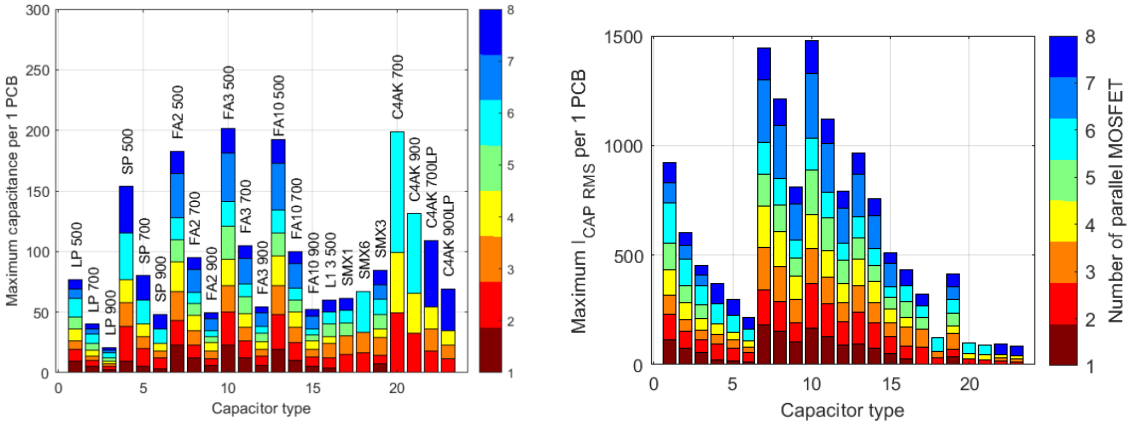


Figure 103 – Maximum total capacitance and RMS current per PCB

Final figures for DC-link volume under different switching frequencies and phase current are presented in Figure 104. Target DC-link voltage is 400V to show the maximum variety of capacitors, and capacitors with lower voltage show better results, therefore only they (one type from each series) are included in the results set. The results for higher voltage do not change much as the decrease in required total capacitance at higher voltage

(see Figure 97) is compensated by a decrease in maximum capacitance of a single capacitor (see Figure 103). It is noticeable that change in frequency affects all types in similar way and causes slow increase in the required volume. By contrast, an increase in the phase current demands a faster rise of volume for film and X7R capacitors due to the low value of maximum RMS current.

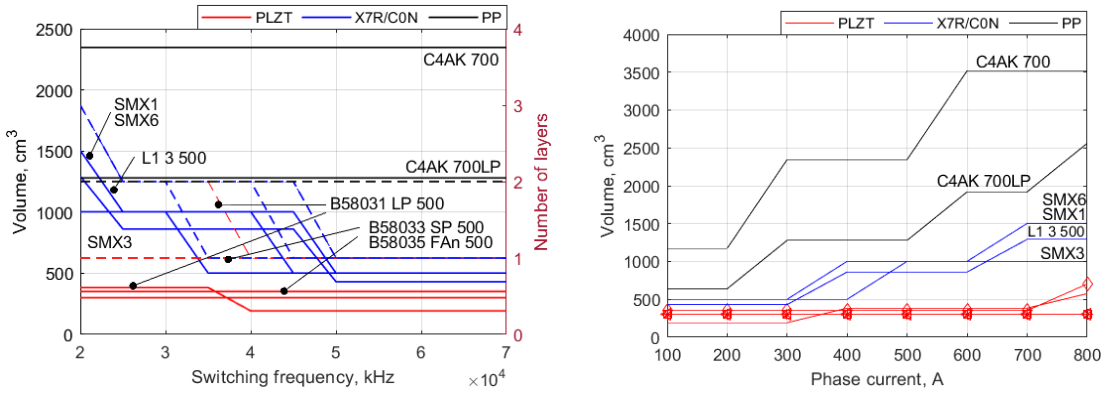


Figure 104 – Volume of DC-link capacitor bank for various switching frequency and phase current (solid line – volume, dash line – the number of PCBs, M=1, V=400V)

Conclusion:

- The volume of DC-link capacitors varies in a wide range in dependency on their types, switching frequency, phase current and modulation characteristics of the inverter. For most ceramic capacitors the minimum expected volume could be from 0.5L to 1.5L. Film capacitors have 2-2.5 times higher volume due to limited RMS current.
- Utilization of high switching frequency and high DC-link voltage could help to reach higher values for power densities.
- Usage of ceramic and film capacitors together is a promising solution to straighten weak points of each type and reach acceptable combinations of total capacitance, volume, the efficiency of space utilization and price if some optimization function is applied. Further research with more accurate models for capacitors and “packing problem” solver for different PCB shapes is required.

Table 22 – HT HV DC-link capacitors

Type	Material	Voltage, V	Capacitance, µF	I_{RMS10K}, A	Temperature, ℃	Dimensions, mm
B58031 LP	PLZT	500/700/900	0.6/0.25/0.13*	2.6/1.6/1.5	150	7.8x7.1x4
B58033 SP	PLZT	500/700/900	12/5/3*	16/12/5	150	33x22x11.5
B58035 FA2	PLZT	500/700/900	1.2/0.5/0.26*	2.5/3/2.5	150	6x7.4x9
B58035 FA3	PLZT	500/700/900	1.8/0.75/0.39*	5/4/3	150	9x7.4x9
B58035 FA10		500/700/900	6/2.5/1.3	13/10/5	150	30x7.4x9
L1 3	C0G	500	2	10	200	25x12.7x15.2
SMX1	X7R	500	8.2	17	200	52x12.7x18.5
SMX6	X7R	500	27	24	200	52x31.8x18.5
SMX3	X7R	500	3,9	7,2	200	26.7x11.4x18.5
C4AK	PP	700/900	60/40	24/22	135	57.5x35x50
C4AK LP	PP	700/900	22/14	15/14	135	42x43x25

3.9 Chapter Summary

According to the results of the comparative analysis, in low-power applications (up to 50kW), both SMT and THT discrete devices show the same performance as power modules. However, THT devices and power modules only would be the preferable choice for high-power applications. For HT applications, restrictions on the case temperature of power modules noticeably limit maximum coolant temperature and maximum output power, and discrete elements do not have such limitations. As expected, the most recent types show significant improvement in thermal performance and output power by comparison with old ones within the same package and dimensions. So inverter performance could be improved merely by replacement of older devices with new ones without modifications of layout, PCB structure etc.

The thermal model complemented by the dataset of 30kW PMSM and the cold plate model is used to calculate the power densities of the complete IMD with various types of SMT MOSFETs. The square shape of the inverter shows a higher density of MOSFET layout than the round one; therefore, it is the preferable choice if the system structure does not apply other restrictions (e.g., shaft extension, encoder presence, etc.). For the given power level, machines' characteristics, and IMD structure, the maximum achievable gravimetric and volumetric power densities are 6 kW/kg and 16 kW/L. PE mainly contributes to the volume of IMD occupying 50-75% of total space, and MOSFET characteristics significantly affect the performance and dimensions of the inverter.

The DC-link capacitor bank for HT application usually occupies a significant part of IMD's inner space, and the proposed method can size its volume, number of components, etc. According to the calculation results, the highest density is achieved with modern PLZT capacitors, although a significant quantity of capacitors is required to achieve the required capacitance. Evaluation of PCB quantity for each type of capacitor shows that for typical low and middle power applications, a single square PCB of about 200cm2 can accommodate the necessary number of capacitors. Low switching frequency or high phase current lead to a substantial increase in minimum DC-link capacitance.

Chapter 4

4 Theoretical analysis of crosstalk signals in parallel connection of switching devices and gate driver adopted for this connection.

4.1 Negative consequences of fast switching process

Over the last two decades, the continuous improvement of new semiconductor materials has greatly contributed to the popularity and variety of SiC power devices. Power converters made a big step toward higher power densities, higher switching frequencies, and lower losses due to SiC outstanding characteristics[84, 93]. With fast switching transient processes, SiC MOSFETs can operate at a higher switching frequency without deteriorating system efficiency. Therefore, weight optimizations of the cooling system and power filters are possible leading further towards the converter's miniaturization[94].

Although power electronics are prospering these days, conquering transportation and aviation confidently, the engineers experience new issues which are, in fact, downsides of SiC incredible performance[95]. Fast switching and high maximum drain-source voltage led to extreme values of voltage rate, and a short pulse of current with significant magnitude is injected through reverse transfer capacitance into the gate circuit when drain-source voltage changes from one extremum to another. Although the mechanism generating the pulse exists in all types of MOSFETs regardless of their material, SiC devices suffer the most. If unaddressed, the generated voltage can easily reach the threshold level and cause the shoot-through or the thermal runaway[96]. To increase the margin between threshold level and gate voltage in a turn-off state, the negative shift of minimal gate voltage became a rule of thumb if SiC devices are used in the design.

Though negative gate voltage helps in the majority of applications, there are still special cases (e.g., unusually high rates of V_{ds}, high ambient temperature), where the safe margin is not big enough and additional measures are required to prevent spurious turn-on. A large number of researchers studied this phenomenon, focusing on methods to evaluate or predict the level of generated voltage [97], [98] and methods to reduce its amplitude. Some methods exploit separated turn-on and turn-off resistance (or modify them) to clamp gate voltage tightly to gate driver output[99], [100], [101]. The schematics of these gate drivers are simple and usually do not need additional control signals. The direct proportion

between the rate of V_{ds} and suppression efficiency is a feature of such structures, and it could be considered as a drawback for some applications. Another approach is an adaptive shift of gate voltage that can temporarily change voltage levels to satisfy safe conditions [102], [103]. The gate driver circuit includes a sophisticated system of sensors and switches to perform shift operations.

Although the problem is well covered for the case of a single device, there is a lack of solutions for parallel MOSFETs, and SiC MOSFETs connected in parallel are still exposed to high $^{dV_{ds}}/_{dt}$. Meanwhile, the parallel connection has several distinct features which limit the efficiency of the solutions suitable single MOSFET. First, several MOSFETs demand higher total gate current, therefore, there could be no room for centralized clamp techniques with no or low turn-off resistance due to limited maximum gate driver current. Second, the parallel connection has non-zero trace parasitic inductance due to spread gates' locations. That inductance limits $^{dI}/_{dt}$ of bypassing circuits (clamps), thus, reduces its efficiency. The third concern is that sometimes the gate circuit experiences a limit of free space, and its PCB cannot accommodate many additional components if a complex auxiliary circuit is implemented for each MOSFET of the group.

The chapter presents a gate driver for a parallel MOSFET connection with an auxiliary clamping to reduce crosstalk between devices in leg configuration. The circuit works independently of the main gate driving circuit and does not affect switching times. Also, the loop path for crosstalk current is in the vicinity of its MOSFET, so parasitic inductances have less influence on the performance of the clamp. The simulation model of $V_{ds}(t)$ based on gate charge current and accurate C_{rss} calculation is developed to analyze generated gate voltage and efficiency of suppression circuits.

4.2 Modelling of crosstalk for parallel connection of MOSFETs

A) Gate drive circuit with parallel MOSFETs

The design of a gate driver circuit is challenging due to distributed gate inputs' locations. Moreover, stable operation of parallel MOSFETs requires individual gate resistance for each transistor that makes it difficult to use conventional methods of crosstalk suppression. Dimensions of MOSFET's package usually determine distances between gates. Parasitic trace inductance between the gate driver and the farthest gate always exists and could affect the gate signal significantly in case of a high inductance value.

An example schematic of a distributed gate drive circuit and its simplified model are presented in Figure 105. Figure 106 shows the inverter prototype with a switching group of parallel SiC MOSFET and its gate driver's traces.

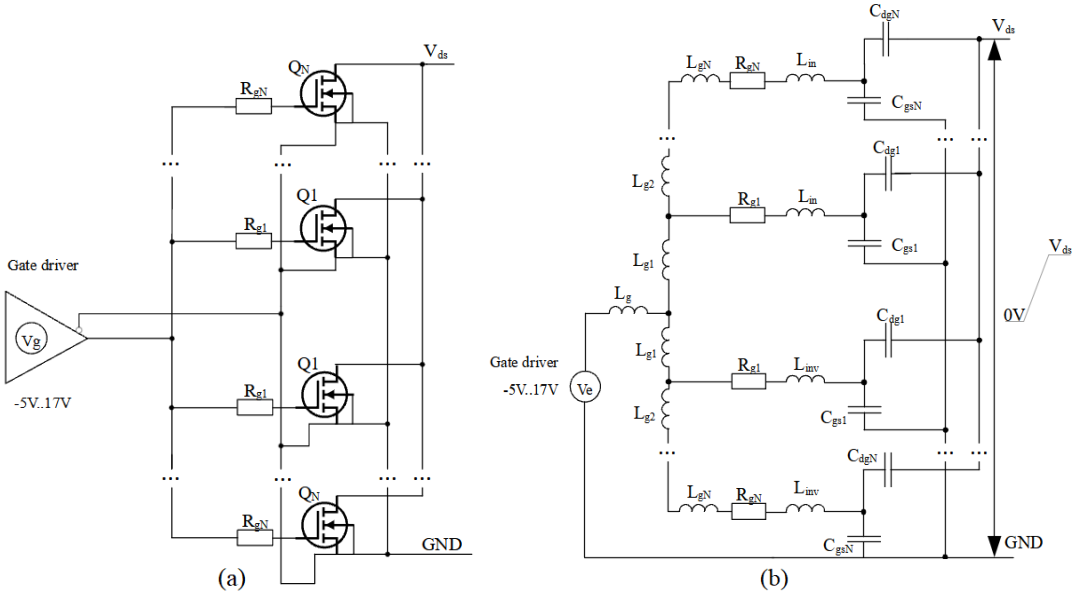


Figure 105 – Schematic of a distributed gate drive circuit (a) and its simplified model (b)

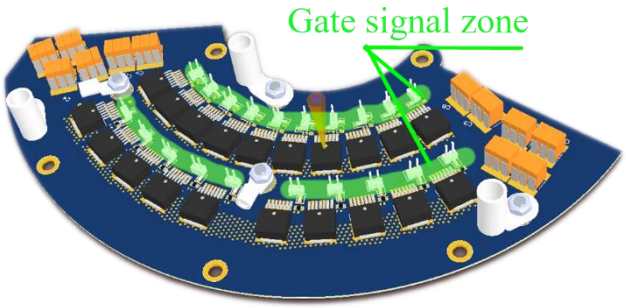


Figure 106 – Example of parallel MOSFET (10 in a group) and layout of gate traces.

The model is considered symmetrical with respect to the centre of the MOSFET group, so the output of a gate driver bifurcates into two equal branches at the line of symmetry. In this case, voltages and currents are the same in the two branches (considering all components have equal values). The model also assumes that all MOSFETs have the same characteristics and parasitic elements. The model is suitable for MOSFETs with separated source pin that conducts only gate signal (TO-263-7 or TO-247-4) as the source parasitic inductance and the transient of drain current are not included into the calculation. The equivalent scheme of the gate circuit for N parallel MOSFETs with gate currents and voltages is presented in Figure 107. Each MOSFET and its gate resistor act as an individual input for the current I_{dg} through MOSFET's reverse transfer capacitance C_{dg}.

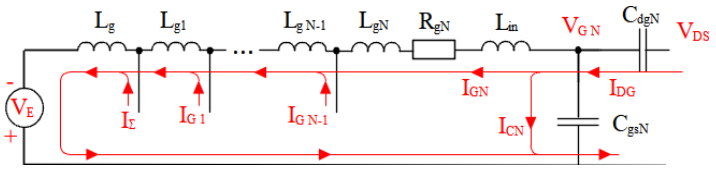


Figure 107 – A single element of a gate driver circuit.

A system of two differential equations expresses the gate voltage (V_{gs}) and gate resistor's current (I_g) for each element with the number $k, 1 \le k \le N$:

$$\begin{cases} V_{Gk} = L_{in}\dfrac{dI_{Gk}}{dt} + \left(R_{g\,inner} + R_{g\,ext}\right)I_{Gk} + \sum_{i=1}^{k}\left[L_{gi}\sum_{j=1}^{N}\dfrac{dI_{Gj}}{dt}\right] + 2L_g\sum_{j=1}^{N}\dfrac{dI_{Gj}}{dt} - V_e \\ C_{dg}(V_{ds})\dfrac{dV_{dg}}{dt} = I_{Gk} + C_{gs}\dfrac{dV_G}{dt} \\ V_G(0) = -V_e;\ I_{Gk}(0) = 0; \end{cases}, \quad (41)$$

where R_{gin} and R_{gex} are inner and external gate resistances ($R_{gin} + R_{gex} = R_g$). The parasitic inductance L_{in} includes both inductance of MOSFET leads and inductance of traces between the main gate signal trace and the gate. The exact value for lead's inductance could be obtained from the manufacturer's SPICE models, and, in general, the value of about 15nF is a good estimation for this parameter.

Other trace inductances are calculated regarding trace shape, structure, and materials of PCB. The equation for the inductance of PCB trace made of 2 parallel strips with a dielectric between and for inductances of 2 parallel wires with opposite current are follows:

$$\mathcal{L}_{PCB} = \frac{\mu_0\mu_r HL}{W},\ L_{2wire} = \frac{\mu_0 L}{\pi}\left(\ln\left(\frac{2D}{d_{wire}}\right) + \frac{1}{4}\right) \quad (42)$$

where μ_0, μ_r are the permeability of free space and relative permeability of PCB material respectively; L, W, H are length, width of the trace and distance between layers respectively; D, d_{wire} are the distances between wires and their diameter. Values of trace inductances with various parameters are presented in Figure 108

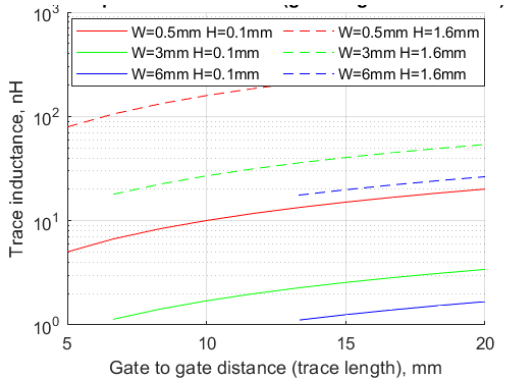


Figure 108 – Gate-to-gate trace inductances with different lengths, widths, and PCB

thicknesses.

According to the results, in some cases inductance of traces between the gate driver and the gate resistor is comparable with an inductance of MOSFET leads. Figures for further model simulation are shown in Table 23.

TABLE 23 - Trace parameters and inductance values

Gate to gate distance (L), mm	Layer thickness (H), mm	Trace width (W), mm	Relative permeability	Gate to gate inductance (L_{gk}),nH	Common path inductance (L_g), nH	MOSFET lead's inductance, (L_{in}), nH
12	0.1	4.5	4	1.34	10	15+6.5

B) Crosstalk during the forced rise of drain-source voltage

The change of drain-source voltage V_{ds} is a reason for the crosstalk gate signal, so the behaviour of V_{ds} determines the shape of injected gate current I_{dg} and gate voltage (V_{gs}) during the crosstalk. In a real device many factors influence the transient of V_{gs} and increase the complexity of the modelling process. The parasitic inductances of the drain circuit, charging of the output capacitor, and reverse recharge of the body diode are not included in the calculation to focus on processes in the gate circuit. Influence of those factors is described at the end of the chapter. Considering there are no parasitic components across the power connections between high and low sides MOSFETs, DC link voltage could be expressed as:

$$V_{DC\ link} = V_{ds\ HS} + V_{ds\ LS} \rightarrow V_{ds\ LS} = V_{DC\ link} - V_{ds\ HS} \tag{43}$$

According to the basics of MOSFET switching with inductive load, $V_{ds\ HS}$ starts to decrease with the rate that is proportional to gate current $i_{gHS}(t)$ when V_{gsHS} reaches level of Miller plateau (V_{GDMill}):

$$V_{dsHS} = V_{dgHS} + V_{gsHS} = \int_{tstart}^{t1} \frac{-i_{gHS}(t)}{C_{dg}(V_{dsHS})} dt + V_{GDMill}, V_{dgHS}(t_{start}) \tag{44}$$

$$= V_{DC\ link} - V_{GDMill}$$

$$i_{gHS}(t) = \frac{V_{gmax} - V_{GDMill}}{R_{gin} + R_{gex}} \tag{45}$$

V_{GDMill} could be obtained through threshold voltage (V_{th}), maximum drain current (I_{max}), and forward transconductance (g)

$$V_{GDMill} = V_{th} + gI_{max} \tag{46}$$

In this study SiC MOSFET NVBG020N120SC1 is used, its characteristics are presented in Table 24.

TABLE 24 - Characteristics of NVBG020N120SC1

Input gate capacitance, pF	Threshold voltage, V (Id=10mA)	Forward transconductance, S	Gate resistance, Ohm	Maximum gate voltage, V
2943	2.7	34	1.6	25/-15

Although these data are clearly stated in the datasheet, figures must be adjusted to the operational point because of the high non-linearity of transconductance characteristics. Transfer characteristics are presented in Figure 109. Datasheet table values for transconductance and gate threshold voltage are 34A/V and 2.7V respectively, and adjusted values (to the point of $I_{max} = 40A$) are 24.6A/V and 6.96V.

$$V_{GDMill25℃} = V_{th25℃} + g_{app25℃} I_{max} = 6.96V + 24.6\frac{V}{A}40A = 8.59\,V \qquad (47)$$

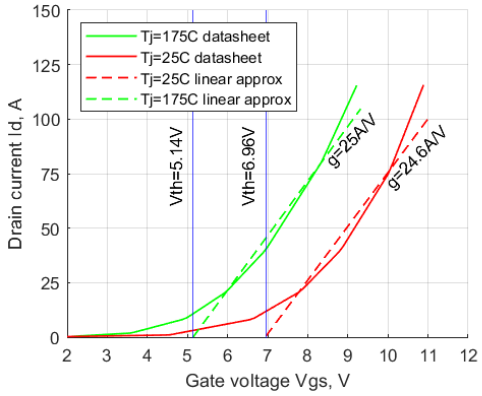


Figure 109 – Transfer characteristics and its linear approximation at different junction temperatures

The drain-gate capacitance or reverse transfer capacitance (C_{dg} or C_{rss}) is a function of Vds and cannot be used directly as a constant value. Instant value of $C_{dg}$is calculated with *Matlab* by 2-step (linear and logarithmic) approximation of datasheet plot. In the first step, several points are acquired manually from the datasheet plot with the software *GetData Graph Digitizer*, so linear approximation fits the required curve in log axis. Then logarithmic approximation in *Matlab* is used to transform copied linear approximation of log curve into normal linear approximation by calculating the following coefficient for each interval:

$$m_i = \frac{log_{10}(\frac{C_{rss\,i+1}}{C_{rss\,i}})}{log_{10}(\frac{V_{ds\,i+1}}{V_{ds\,i}})}. \qquad (48)$$

Additional points can be obtained by applying this coefficient to any value of V_{ds} within the range ($V_{ds\,i}$; $V_{ds\,i+1}$) into the equation:

$$C_{rss\ j} = C_{rss\ i}\left(\frac{V_{ds\ j}}{V_{ds\ i}}\right)^{m_i} \tag{49}$$

Both approximations are added to the datasheet's plot (see Figure 110) so that difference could be observed.

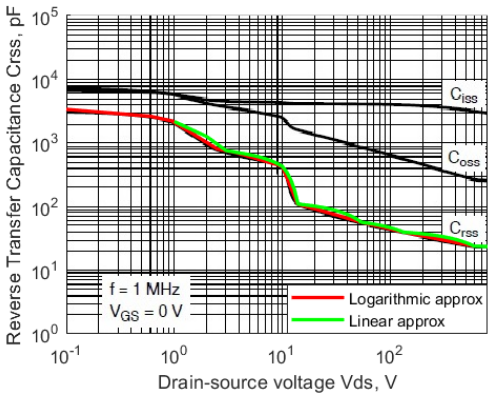


Figure 110 – Comparison of logarithmic, linear approximations, and datasheet curve[104].

With a significant number of additional points, it is possible to use look-up tables with linear approximation to accurately find intermediate points during the numerical calculation process. Simulink model of V_{ds} voltage source is presented in Figure 111.

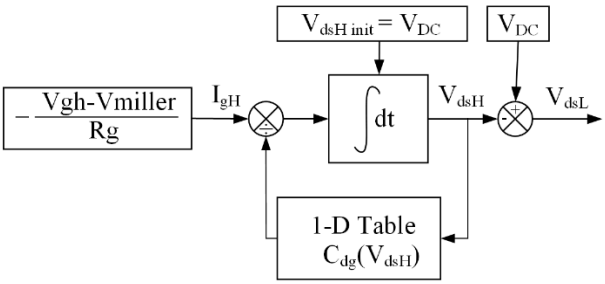


Figure 111 – Simulink model of the voltage source to imitate V_{ds} behavior.

Another approach to determine the instant value of V_{ds} is to use a ramp voltage source with $dV_{ds\,HS}/dt$ calculated through total charge of $C_{dg}(V_{dg})$ that is required to discharge the capacitor from initial $V_{ds} - V_{GDMill}$ to the beginning of the ohmic region $V_{ds\,min}$.[98]

$$V_{ds\,min} = I_{max} R_{d\,on}(V_{gs} = V_{GDMill}) \tag{50}$$

$$Q_{dg\,sat} = \int_{V_{ds\,min}}^{V_{ds\,max} - V_{miller}} C_{dg}(V_{ds})\, dV \tag{51}$$

Switching time t1 is determined by both charging capabilities of the gate driver circuit and drain-gate capacitance of MOSFET and calculated by:

$$t_1 = \frac{Q_{dg\,sat}(V_{dg\,max}, V_{dg\,sat})}{I_g} = \frac{Q_{dg\,sat}(V_{dg\,max}, V_{GDMill})}{\frac{V_{gmax} - V_{miller}}{R_{gin} + R_{gex}}} \tag{52}$$

In absence of parasitic elements, dV_{ds}/dt could be presented as a constant value, therefore $V_{ds}(t)$ has ramp shape starting from 0V and reaching its maximum value $V_{ds\,max}$ at time t_1. Due to the low value of C_{rssHS} at the beginning, the charging process is faster with the same amount of current, and the dV_{ds}/dt is higher with the integration approach, therefore the current pulse through C_{rss} of low side MOSFET is higher (see Figure 112). In further simulations this method is used to generate $V_{ds}(t)$.

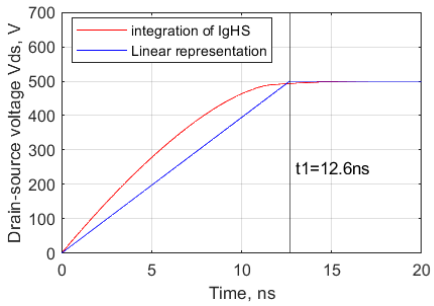


Figure 112 – Drain-source voltage generated by 2 different approaches.

Although the parasitic components of drain and source circuits are omitted in this model, they affect the waveform of both V_{ds} and V_{gs}. The parasitic inductance of the power lines (drains, sources of both high and low sides MOSFETs, and traces between them) causes the voltage overshoot of $L_{par}\frac{dI_d}{dt}$. In this case I_d includes load current, reverse recovery current and charge current of output capacitance. The overshoots extend the period of non-zero dV_{ds}/dt, therefore it increases injected charge and total value of V_{gs}, though the rise is not significant even with noticeable overshoot due to the low value of C_{rss} at high voltage. After the transition of V_{ds} the inductance starts to resonate together with C_{DS} passing the oscillation into gate circuit as well.

The output capacitance of MOSFET and the reverse recovery process affect the MOSFET at forced transient of V_{ds} by generating a short current pulse with significant amplitude. That pulse is responsible for oscillation in the drain circuit (as was mentioned before) and can distort the external gate signal if any common inductivity between the gate and the source (even in presence of Kelvin connection) exists. Common inductance creates an additional voltage pulse in the gate circuit, increasing the load for the gate driver and suppressing circuits.

C) Crosstalk simulation

In case design the simulated model includes 6 MOSFETs in total, per 3 in each branch. Parameters of traces are specified in Table 23. MOSFETs are NVBG020N120SC1.

Simulations are performed in *Matlab* Simulink by numerical solving of differential equations (44) for each MOSFET of 1st branch. Waveforms of simulated crosstalk-generated signals are presented in the figure. Two effects related to parasitic inductance take place there (see Figure 113):

- a small increase in the amplitude of the crosstalk pulse with distance from the central point;
- higher parasitic inductance of gate driver traces leads to a longer oscillation process and, therefore, a longer duration of the main pulse.

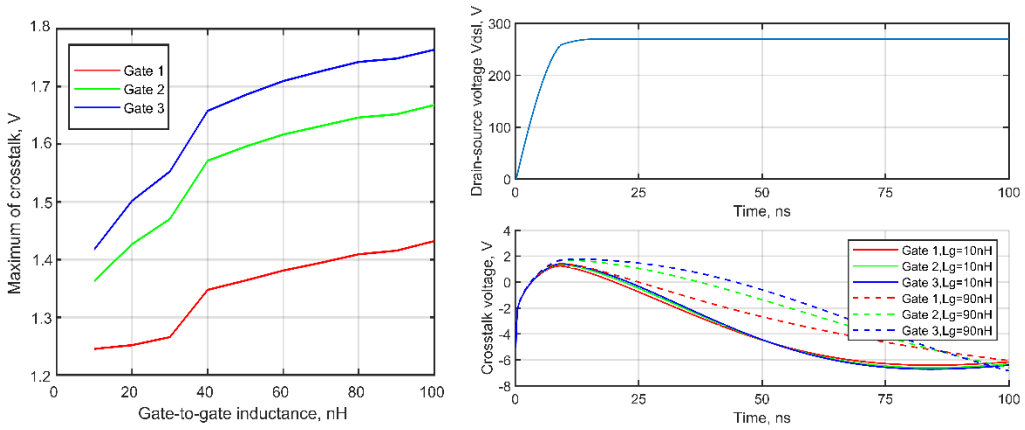


Figure 113 – Behaviour of crosstalk maximum for different gates and different trace inductance (R_{gex}=5 Ohm, V_g=+17V/-5V, I_d=40A, T_j=25ºC).

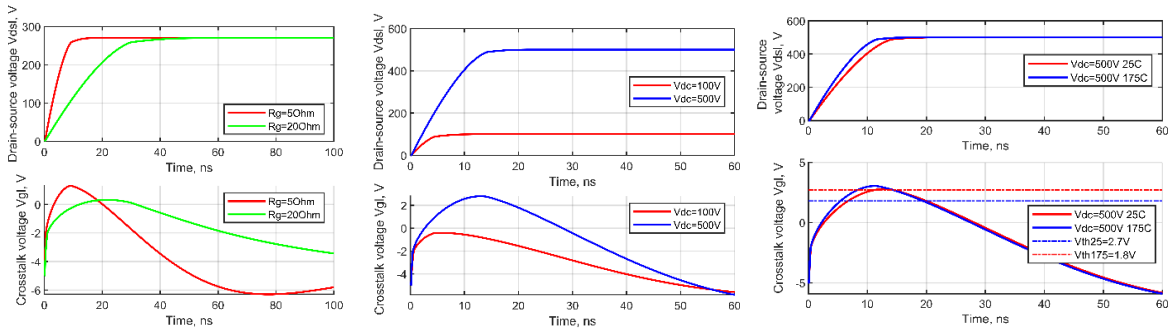


Figure 114 – Crosstalk pulse with different gate resistance, drain voltage, and temperature (default conditions are R_{gex}=5Ohm, L_g=5nH, V_g=+17V/-5V, I_d=40A, T_j=25ºC).

According to the results (see Figure 114), a spurious partial turn-on is possible with high voltage (>400V) and high junction temperature. Therefore, suppressing measures to reduce crosstalk should be applied to avoid excessive power losses and MOSFET thermal destruction.

The results show that a smaller value of the gate resistor does not help to decrease the crosstalk but makes the pulse even higher. Although low R_{gex} can drain a higher amount of injected current from the gate, it also increases the rate of V_{ds}at the turn-on/turn-off and,

in turn, the amplitude of the injected current. The situation could be improved if a second gate resistor is added to the gate circuit to separately discharge the gate and to prevent the increase of $^{dV_{ds}}/_{dt}$ at the turn-on. The drawbacks are higher parasitic inductances of the gate circuit (two lines share the same area of PCB) and higher $^{dV_{ds}}/_{dt}$ at the turn-off. Latter results in higher ringing amplitude and might cause a problem with EMI compatibility on the inverter level[84]. Moreover, fast discharge requires higher current capability of the gate driver that could be not acceptable in a parallel configuration.

It is worthwhile to notice that there is no method to remove the crosstalk entirely due to non-zero resistance and inductance inside the MOSFET package. In case of an ideal connection between the transistor and an ideal gate power supply, a voltage is still generated between the gate and the source, though the voltage is undetectable for external measurements, and could be evaluated by the rate of V_{ds} only (see Figure 115).

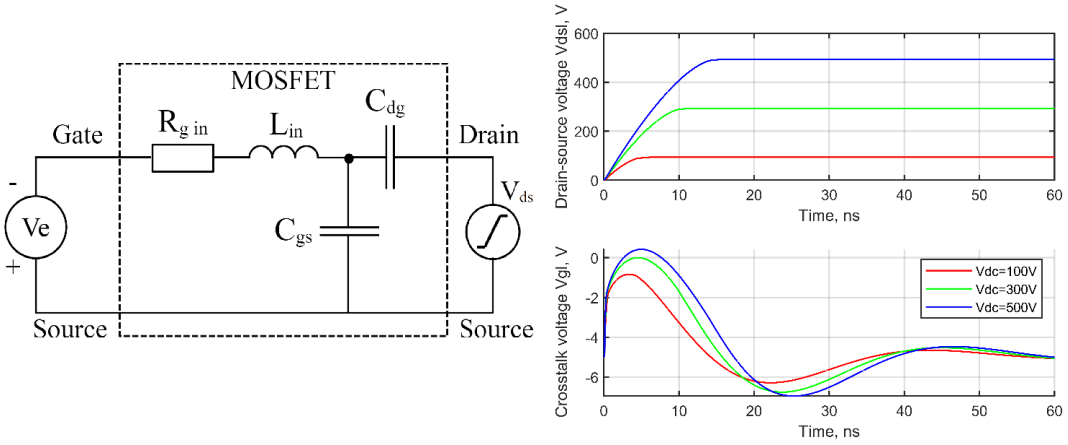


Figure 115 – Inner gate voltage during crosstalk with shorted gate circuit (LS gate pin is shorted with V_e, HS gate has 5Ohm external resistor)

4.3 The gate driver design with crosstalk suppression.

A) Design considerations

The requirements for a new gate driver circuit are following:

- Does not change the output current of the gate driver or change the switching time.
- Effectively suppresses positive and negative crosstalk.
- Simple circuit due to limited space and a large number of parallel MOSFETs.
- Does not connect all gates to the same point directly as it might cause the stability problem.

The simplest possible solution is to add another transistor that clamps the gate to the minimum voltage of the gate driver. The schematic of the driver is presented in Figure 116. The control signal of HS switches is used to control Q_{FN}; therefore, a second channel is required for isolation IC. The transistor Q_{FN} is on during the turn-on of the high-side MOSFETs, and the current I_{dg} is shorted through Q_{FN} to the minimum value of gate voltage. Although Q_{FN} is switched off before V_{ds} starts to decrease again, the current I_{dg} generated with C_{rss} is shorted by the body diode of Q_{FN}. The transistor Q_{FN} is already off at the switching of Q_N and does not affect its transient time providing freedom to choose gate resistance independently. Waveforms of voltages and currents are shown in Figure 118. In theory, the voltage V_{gs} is lower as R_{gN} is bypassed during the transient of V_{ds}. The amplitude of the crosstalk pulses mostly depends on the value of parasitic inductance between Q_{FN} and power supply output. Considering that both gate trace and this additional "-5V" trace share the same area, it is really challenging to keep total trace inductance for all MOSFETs below 15-20nH. Simulation (results in Figure 123) shows that high trace inductance cancels any advantages of skipping R_{gN} and increases oscillation of V_{gs}.

The proposed driver is based on [105] designed for a single transistor structure. The schematic of the proposed driver is presented in Figure 117. A capacitor C_{FN} is added to the gate driver circuit, so current I_{dg} is shorted through C_{FN} and Q_{FN}. During the turn-off period, C_{FN} is charged to the minimum voltage of the gate driver with respect to source potential, therefore, V_{gs} is clamped at the minimum of gate voltage. In that case, there is no need for a separate power line as it is for the scheme in Figure 116. The amplitude of crosstalk pulses depends on the capacitance of C_{FN} and the on-state resistance of Q_{FN}. Waveforms of voltages and currents are shown in Figure 118.

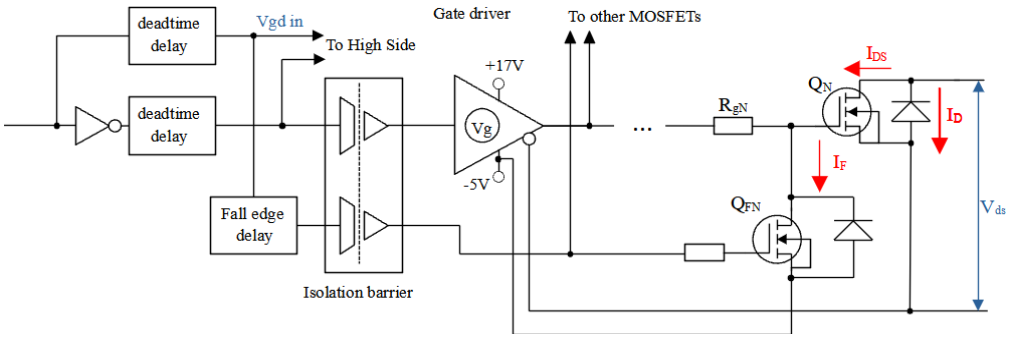


Figure 116 – Structure of a driver with external clamping.

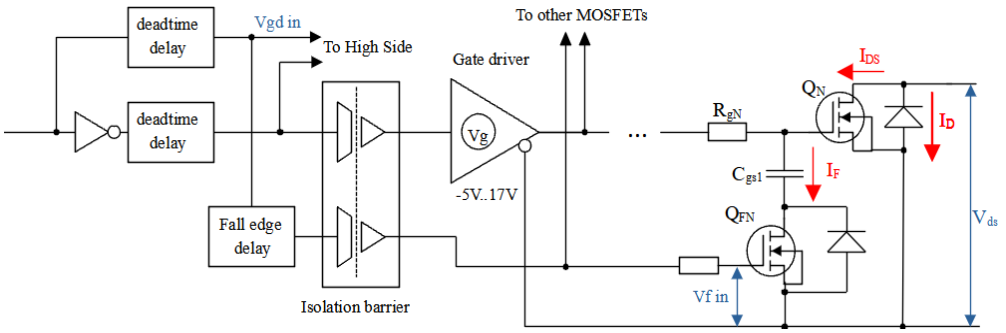


Figure 117 – Structure of proposed gate driver.

The fall edge delay could be added in order to shift Q_{FN} turn-off and use its low-ohmic channel in parallel with the diode to suppress negative crosstalk current.

The circuit should be connected as close as possible to the gate input of power MOSFET. Although its efficiency is not affected by the parasitic inductance of traces between MOSFET and the gate driver, inductances between C_{FN}, Q_{FN}, Q_N limit the amplitude of the shorted current.

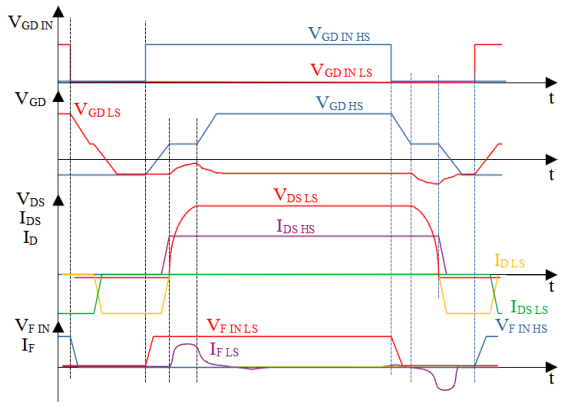


Figure 118 – Waveforms of voltages and currents during a single cycle.

The equivalent circuit of the proposed driver for one of the parallel MOSFETs is in Figure 119. The Transistor Q_{FN} could be replaced with its on-state resistance R_F. Transistor Q_N has inner gate resistance $R_{g\ in}$ and inductance L_{in} that are connected in series with shunt circuit and, therefore, they reduce the efficiency of suppression.

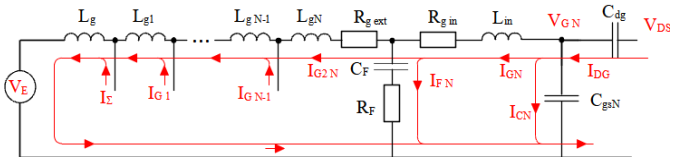


Figure 119 – Equivalent circuit of gate circuit

For each MOSFET's gate circuit a system of differential equations could be determined:

$$\begin{cases} V_{fk} = R_{gext} I_{g2k} - R_f I_{fk} + \sum_{i=1}^{k} \left[L_{gi} \sum_{j=1}^{N} \frac{dI_{g2j}}{dt} \right] + 2L_g \sum_{j=1}^{N} \frac{dI_{g2j}}{dt} - V_e \\ V_{gk} = L_{in} \frac{dI_{gk}}{dt} + R_{gin} I_{gk} + V_{fk} + R_f I_{fk} \\ C_{dg}(V_{ds}) \frac{dV_{dg}}{dt} = I_{gk} + C_{gs} \frac{dV_{gs}}{dt} \\ I_{gk} = I_{fk} + I_{g2k} \\ V_{gk}(0) = V_{fk}(0) = -V_e;\ I_{gk}(0) = I_{g2k}(0) = 0; \end{cases} \tag{53}$$

The numerical solution of the system is performed by *Simulink/Matlab* using the same voltage generator for $V_{ds}(t)$ based on the integration of I_{gHS}. Figure 120 shows a comparison between proposed and conventional drivers. The new driver reduces the amplitude of crosstalk significantly and almost eliminates the difference in its amplitude for all parallel MOSFETs.

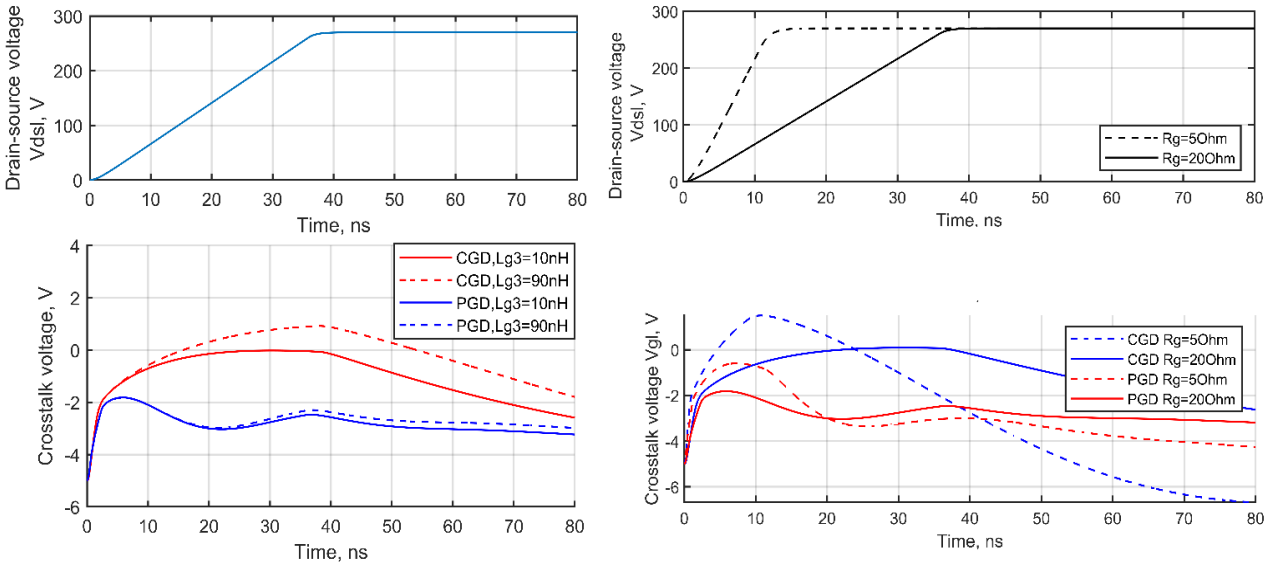


Figure 120 – Comparison of proposed gate driver (PGD) with conventional driver (CGD) with different component values and voltage.

The proposed gate driver helps to maintain V_{gs} below the threshold level with a reasonable level of negative voltage shift, though it cannot eliminate the crosstalk entirely. Comparing Figure 121 and Figure 114 one could easily notice that V_{gs} has almost 2V margin toward the threshold with auxiliary circuit, although V_{gs} exceeds that level in the previous configuration.

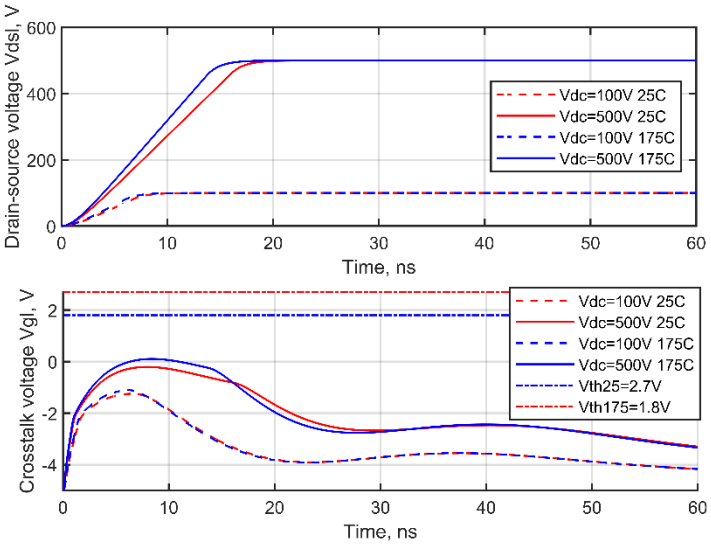


Figure 121 - Crosstalk pulse with different gate resistance, drain voltage, and temperature.

The resistance R_f and C_f form a buffer (or short path) for I_{gs}, and their values determine the efficiency of the circuit. A too small capacitor cannot absorb current pulse without a noticeable increase in voltage, and too high on-state MOSFET's resistance merely reduces shunt capabilities (see Figure 122). Although there are no principal disadvantages of high capacitance or low resistance, high values of capacitance require larger dimensions of the capacitor and charge current could damage the body diode during initial charging.

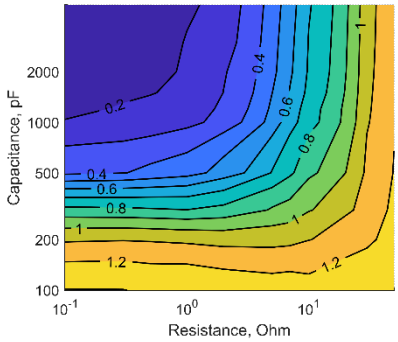


Figure 122 – Maximum gate voltage at crosstalk with different Rf and Cf values (Rg=5Ohm, Vds=270V, T=25°C, $V_{E\ NEG}$=-5V)

In Figure 123, different methods of crosstalk suppression (parameters according to Table 25, transient of drain voltage is recorded and independent from Rg) are compared. Proposed driver provides short individual path for the injected current pulse, therefore, its transient is faster and has lower amplitude than central clamp method with better traces layout (L1).

Table 25 – Parameters for comparison analysis of suppression methods.

Type	External gate resistor Rg, Ohm	Parasitic inductance, nH		Note
		common part	gate part	
No suppression	5	20	12	$R_{G\ INN}$=1.6 Ohm, $L_{G\ INN}$=13 nH, V_E= -5V
Ideally shorted to V_E	0.1	0	0	
Clamped to V_E (type 1)	0.1	5	9	
Clamped to V_E (type 2)	0.1	20	12	
Proposed driver	5	20	12	

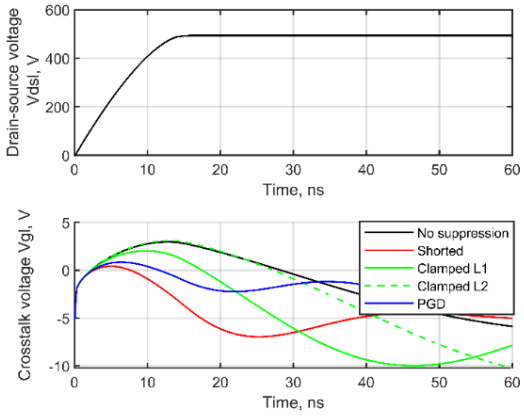


Figure 123 – Crosstalk with different suppression techniques (R_{gexHS} =5Ohm, Tj=25C)

Additional elements increase the overall power consumption of the gate circuit. That power losses include recharging of additional MOSFET's output and reverse capacitances and recharging of its gate capacitance.

$$P = F_{sw}\left(V_{gmax} - V_{gmin}\right)^2 \left(C_{DS\,at} + C_{rss\,at}\right) + F_{sw} {V_{g\,at}}^2 C_{g\,at} \qquad (54)$$

B) Experiment results

To test the proposed method 4 gate driver circuits are modified according to Figure 117 with 2nF capacitor and MOSFET AO3442 (maximum Vds=100V, $R_{DS(on)}$=0.5Ohm). One gate circuit is not modified to have a control sample. Modified circuits are shown in Figure 124. In order to reduce additional consumption, the supply voltage for the modified is reduced to +15V, and it is generated from +17V DC-DC converter of the main GD with a zener diode. The second digital isolator is used to transfer the control signal of the auxiliary circuit.

Figure 124 – Modified gate circuit (additional MOSFETs with capacitors)

The results are presented in Figure 125 and show a reduction in the amplitude of gate

voltage during the crosstalk. The difference in gate voltage between modified and unmodified circuits is about 1V, and it remains the same with Vds in a range from 75V to 275V. Also, the generated gate voltage decreases faster with modified GD and, therefore, the probable length of the shoot-through event is shorter.

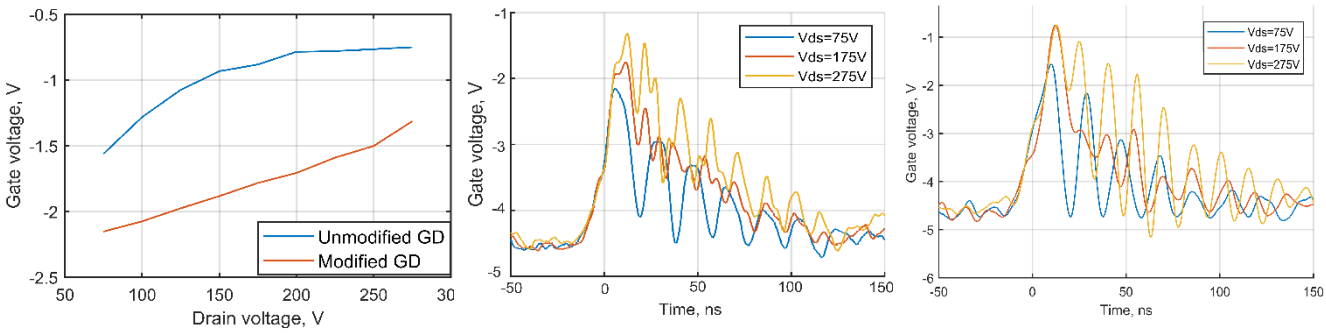


Figure 125 – Comparison of the maximums of gate voltages during crosstalk and their waveforms (R_{gex}=10Ohm, V_g=+17V/-4.5V)

Experimental results demonstrate a good correlation with simulation (see Figure 126). So the model can be used to predict the behaviour of gate voltage during the crosstalk event and evaluate required values for components of the suppression circuit.

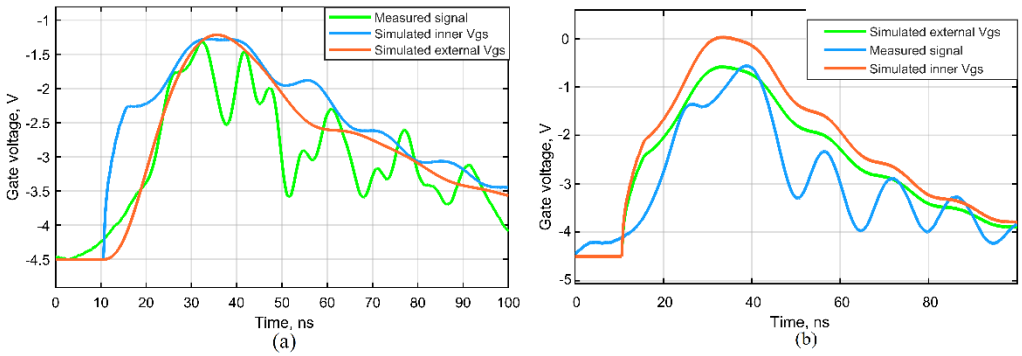


Figure 126 – Comparison of experimental results and simulated results (a – PGD, b - CGD).

Additional power consumption due to recharging of MOSFET's capacitances is calculated with (53):

$$P = 4 * (50kHz(17V + 4.5V)^2(10pF + 10pF) + 50kHz(15V)^2 100pF)$$
$$= 6.3\,mW \qquad (55)$$

4.4 Chapter summary

The results of the simulations show that the negative effect of crosstalk could become noticeable (especially for devices with low threshold voltage) due to short switching time, high Vdc, and high temperature. Spontaneous "turn-on" of the MOSFET could increase switching power losses and additional self-heating of MOSFETs. Additional parasitic inductance between parallel MOSFETs in the range of 10-100 nH has a limited effect on the amplitude of crosstalk voltage, therefore, all MOSFETs experience almost the same level of injected current and induced gate voltage regardless of their position in the group. Lower external gate resistance does not help to reduce injected current from the gate but increases it due to a faster transition of drain voltage. Moreover, the existence of inner parasitic elements in the gate circuit of MOSFET prevents the elimination of the crosstalk voltage pulse. The voltage pulse is generated on the gate even with short-circuit between the gate pins. Therefore, gate voltage shift to the negative area is required to guarantee "open" status during the turn-off period.

Modified GD is proposed to reduce the possibility of unintentional "turn-on" by creating an individual short path for injected current through an additional capacitor. The proposed modification of GD offers a reduction of crosstalk voltage amplitude and pulse duration for both polarities without a significant increase in gate driver power. The circuit also does not occupy much PCB space and does not require wide traces for operation as the high current circulates in the vicinity of the gate. The experiment shows the crosstalk reduction is about 1V for the given MOSFET type and the gate structure.

If better protection against the crosstalk is required, level-shifting circuits could be used at the expense of a noticeable increase of GD power due to additional recharge of the gate capacitance every cycle. In the case of a parallel MOSFET connection, the total required power might reach several watts.

Chapter 5

5 Modifications of commercial current sensor to increased temperature range.

5.1 Current sensor in IMD design

An important part of the motor control system is an AC current sensor (CS) that provides feedback information for the current control loop and often acts as a part of an overcurrent protection scheme. The most popular types of current sensors are listed in TABLE 26.

Table 26 - Characteristics of CS

Type of CS	Advantages	Limitation	Maximum temperature, ºC
Shunt resistor	• Simple implementation	• High power losses • Connected with high voltage lines • Bulky package (for high current) • Requires an amplifier;	275
Integrated shunt	• Simple implementation without the increase in overall size; • Suitable for high current;	• Requires an amplifier; • Connected with high voltage; • Available for limited number of power modules;	-
Open-loop hall current sensor (with busbar)	• Simple implementation and small size (single chip); • Measured current up to 200A; • Isolated;	• Limited current and temperature; • Requires physical connection with the busbar; • Low output power (voltage output with high output resistance);	150 (0-100A) 85 (200A)
Open-loop hall current sensor (core)	• Simple implementation (single block); • Wide range of measured current; • Isolated;	• Limited temperature; • Bulky package; • Low output power (voltage output with high output resistance);	125
Closed-loop hall current sensor	• Simple implementation (single block); • Wide range of measured current; • Isolated; • Current output;	• Limited temperature; • Bulky package; • Relatively high power consumption;	85 (200A)
Open-loop hall current sensor (coreless)	• Simple implementation and small size (single chip); • Wide range of measured current; • Isolated;	• Low output power (voltage output with high output resistance); • Mechanical complexity of layout;	150

Although classical shunt resistors can operate under extremely high temperatures, they could be an appropriate choice only at low phase current due to the significant amount of generated heat in high current systems and bulky packages.

Open-loop CS with an integrated busbar provide a wide range of measured current and

insulation from the primary circuit, but the maximum temperature is limited by 85 ºC for high current versions. A solid package and dense layout reduce the efficiency of any external cooling; therefore, they also do not fit the high-temperature integrated system.

Last three options in TABLE 26 draw interest if HT current measurement is required. Open-loop CS with core became quite popular in traction inverters after introducing a novel design with three phases integrated into a single case. The low power of the output signal is vulnerable to EMI if the signal is transferred with long cables, and special measures (shielding or amplification) might be required. Low power consumption of the assembling makes it possible to operate up to 125 ºC of ambient temperature, which is a good result for the commercial off-shelf device.

Coreless open-loop CSs could be considered the smallest possible solution as they occupy an area of a single chip, but they are known for the complexity of usage. Due to the nature of the measuring method (level of magnetic flux), position, orientation, and external fields affect the output. The special shape of the busbar (it cannot work with cables) and shielding is required for accurate measurements. These factors slowed the popularisation of coreless CS despite the attractive advantages in dimensions and weight. However, further development of the CS relaxed some restrictions to facilitate engineer's work, for example, recently introduced devices with Common-Mode Field Rejection are stated to work without any shielding. Although precise machinery of a busbar and positioning of the chip is still necessary to acquire accurate results, it is a positive trend that inspires to wider utilisation of such devices.

By contrast with all open-loop sensors, close-loop CS have a high power of output signal and they can work under harsh EMI conditions at some distance from the processing circuit. The drawback is a high power losses inside the sensor because inner switches work in linear operation mode with relatively high current. The typical maximum operating temperature does not exceed 85 ºC for the majority of models. At the same time, it is possible to extend the temperature range by additional cooling, and CS LA-150P was chosen to investigate appropriate cooling techniques (its characteristics are in Table 27).

Table 27 - Parameters of LA-150P current sensor

Parameter	Value
Primary nominal RMS current, A	150
Primary current (measuring range), A	±212
Measuring resistance (±15V, ±212A), Ohm	0…30
Conversion ratio	2000
Accuracy (Ta=25ºC), %	0.5
Ambient operating temperature, ºC	85

Current consumption (±15V), mA	10+I_{CS}

5.2 Close loop current sensor structure and its thermal management

The electric scheme of the current sensor is presented in Figure 127. It consists of a hall sensor HW-322B with its power supply circuit (two 1,6kOhms resistors and diode), a signal amplifier LM201, a transistor output amplifier, and a secondary coil. Hall sensor's power supply consumes about 10mA at 30V (0.3W) generating heat on resistors regardless of the measured current. The operational amplifier converts the output voltage of the hall sensor into appropriate base signal for the output transistors. Output current I_{CS} goes through one of the transistors, the secondary coil (L_1), and the measuring resistor R_{meas} that is not a part of the sensor but connected in series with the coil L_1.

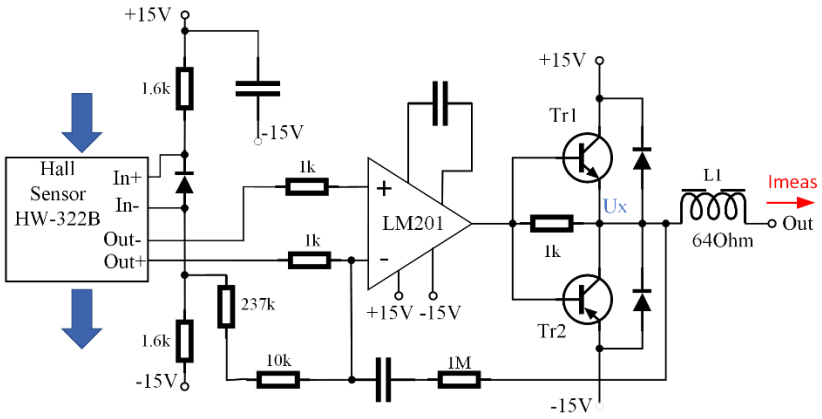


Figure 127 – Schematic of LA-150P LEM sensor.

Considering typical behaviour of phase current (sine waveform and up to 2-3 kHz frequency or constant DC current), power dissipation ($P_{CS\,total}$) of the current sensor includes total power losses of BJTs (P_{BJT}), inductor active losses (P_{coil}) and power supply losses (P_{Hall}). They could be calculated as follows:

$$P_{CS\,total} = P_{BJT} + P_{coil} + P_{Hall} \tag{56}$$

$$P_{BJT} = \begin{cases} \dfrac{2I_{ACmax}V_{dc}}{\pi K} - \dfrac{(R_{coil}+R_{meas})I_{ACmax}^2}{2K^2}, I_{CS} = \dfrac{I_{ACmax}}{K}\sin(\omega t) \\ V_{dc}\dfrac{I_{DCmax}}{K} - (R_{coil}+R_{meas})\dfrac{I_{DCmax}^2}{K^2}, I_{CS} = \dfrac{I_{DCmax}}{K} \end{cases} \tag{57}$$

$$P_{coil} = R_{coil}I_{CSrms}^2 \tag{58}$$

$$P_{Hall} = 2V_{dc}I_{idle} \tag{59}$$

$$P_{BJT\,single} = \begin{cases} \dfrac{P_{BJT}}{2}, & AC\ current \\ P_{BJT}, & DC\ current \end{cases} \tag{60}$$

Power dissipation mainly depends on the RMS amplitude of measured current $I_{AC\,RMS}$

and, to a lesser extent, on the measuring resistance R_{meas} and current waveform (direct or altering). AC current losses of the coil and transistors are comparable as the switches share output current in this case (see Figure 128). By contrast, DC current always flows through one transistor, and its losses jump almost two times.

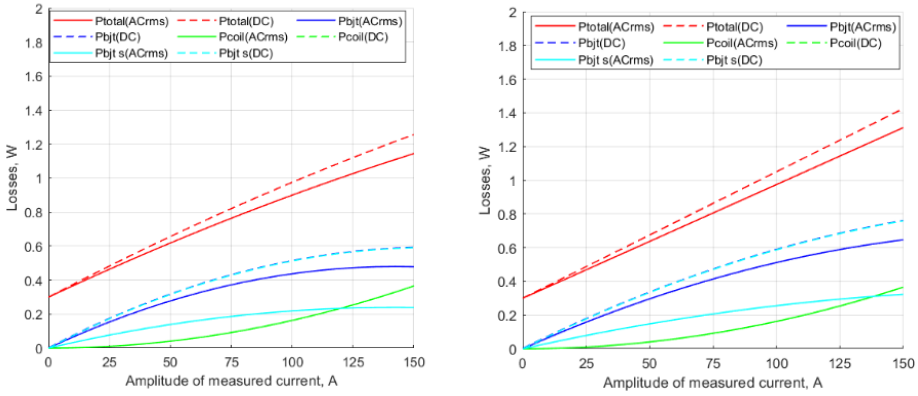


Figure 128 - Power losses of a current sensor with different measuring resistance (left – R=30 Ohm, right – R=0 Ohm)

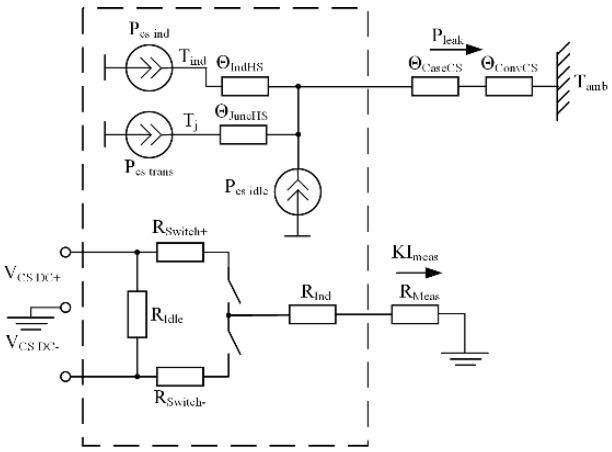


Figure 129 – Thermal model of current sensor.

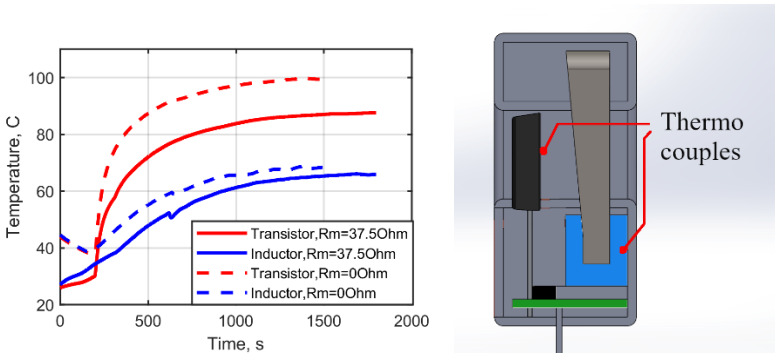


Figure 130 – Temperature of the transistor and the inductor of CS with 37.5 Ohm and 0 Ohm load (input - 150A DC current).

A simplified thermal model of the current sensor is presented in Figure 129. The rise of transistor temperature ΔT_{BJT} and the rise of inductor temperature ΔT_{coil} could be

expressed as follow:

$$\begin{cases} \Delta T_{BJT} = P_{BJT}\Theta_{J-Cs} + \left(P_{BJT} + P_{coil} + P_{HALL}\right)\Theta_{TotCs} \\ \Delta T_{coil} = P_{coil}\Theta_{coil} + \left(P_{BJT} + P_{coil} + P_{HALL}\right)\Theta_{TotCs} \end{cases} \quad (61)$$

Different values R_{meas} result in different power losses in transistors of the current sensor, but inductor and hall sensor losses are the same. Assuming that thermal resistances do not change with temperature, they could be calculated by using experimental results (see Figure 130) with the following equations:

$$\begin{cases} \Theta_{TotCs} = \dfrac{\Delta T_{BJT37.5} - \dfrac{P_{BJT37.5}}{P_{BJT0}}\Delta T_{BJT\,0}}{\left(P_{coil} + P_{HALL}\right)\left(1 - \dfrac{P_{BJT37.5}}{P_{BJT0}}\right)} \\ \Theta_{J-Cs} = \dfrac{\Delta T_{BJT0} - \left(P_{BJT0} + P_{coil} + P_{HALL}\right)\Theta_{TotCs}}{P_{BJT0}} \\ \Theta_{coil} = \dfrac{\Delta T_{coil0} - \left(P_{BJT0} + P_{coil} + P_{HALL}\right)\Theta_{TotCs}}{P_{coil}} \end{cases} \quad (62)$$

Input data for analysis and calculated values are combined in TABLE 28. Given $\Theta_x(\mathrm{T}) = const.$ correlations between transistor and coil temperatures are shown in Figure 131. According to the results, the temperature of the hall current sensor exceeds the maximum acceptable level (110 ºC according to the CS datasheet) with both AC and DC measured current even at the maximum value of the measuring resistor.

Table 28 - Thermal Resistances of the model

Initial parameters		Calculated parameters	
Parameter	Value	Parameter	Value
$\Delta T_{BJT37.5}$, ºC	60.3	Θ_{TotCs}, K/W	27
$P_{BJT37.5}$, W	0.59	Θ_{J-Cs}, K/W	44.8
$\Delta T_{BJT\,0}$, ºC	72.4	Θ_{coil}, K/W	8
P_{BJT0}, W	0.76		
ΔT_{coil0}, ºC	41.2		
P_{coil}, W	0.36		
P_{HALL}, W	0.3		

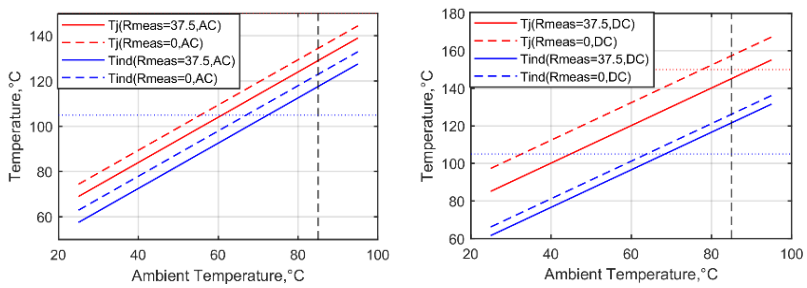


Figure 131 – Transistor and inductor temperatures for AC and DC measured current at different load resistance.

Considerations on capabilities of CS elements to operate with maximum load under high temperature are discussed in TABLE 29. Two types of components (resistors and an amplifier) could be replaced with HT versions, but another three parts need to withdraw generated heat from them to avoid overheating.

Table 29 - Thermal analysis of current sensor's components

Component	Losses, mW	Max operating temperature, ºC	Thermal resistance the still air, K/W	Possible solutions to wide operating temperature range
Hall sensor HW-322B	-	110	Temperature follows inductor's temperature	Remove heat from the coil with a heat sink
Secondary coil	<370	-	≈100-110 (including heat exchange through core's surface)	Remove heat with a heat sink
Operational amplifier LM201	<90	105	≈100	Use LM101 (Tamb<125 ºC); Cooling with a heat sink
Resistors in supply circuit	140	Depends on type (typ. 155)	170-400	Use high power types; Link thermally to cooled components
BJT BD681/BD682	<0.75	150	61	Add a heatsink

5.3 Improvement of sensor's cooling system

The availability of the high-temperature close-loop current sensors (T_{amb}>105 ºC) is quite limited due to their power losses. Relatively high (if compared with open-loop sensors) output current and supply voltage cause noticeable power dissipation on transistor switches and secondary side coil and, in turn, limit maximum ambient temperature. In order to increase the operating temperature range of the commercial current sensor, two solutions of different modification levels are proposed. Both methods exploit a semiconductor thermoelectric cooling module (TEM) to maintain the temperature below the maximum level.

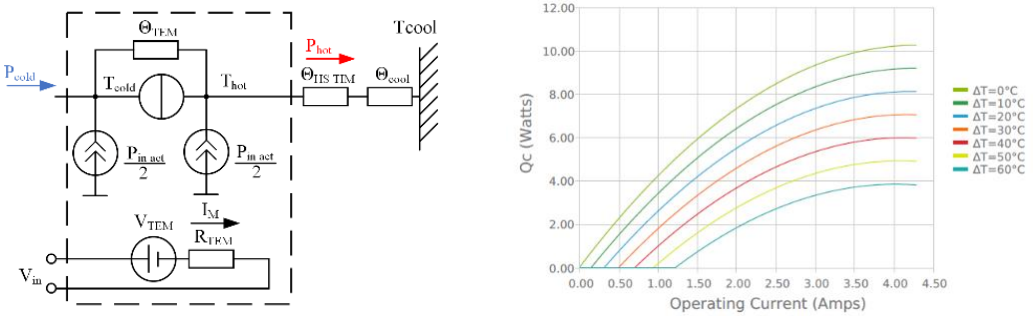


Figure 132 - Thermal model of TEM and its cooling performance.

Thermal model of TEM is presented in Figure 132 (the model is created according to [106]).Voltage V_m applied to the input of TEM determines the pumping performance of the module. Relationships between power P_{COLD} being pumped from the cold side,

temperatures of both sides (T_{HOT}, T_{COLD}), and dissipated power P_{HOT} are described through a system of equations:

$$\begin{cases} V_M = \alpha \Delta T_M + I_M R_M \\ P_{HOT} = \alpha T_{HOT} I_M + \frac{I_M^2}{2} R_M - \frac{\Delta T_M}{\Theta_M} \\ P_{COLD} = \alpha T_{COLD} I_M - \frac{I_M^2}{2} R_M - \frac{\Delta T_M}{\Theta_M} \\ T_{HOT} = P_{HOT} \Theta_{TIM} + \mathrm{T}_{AMB} \end{cases} \quad (63)$$

where α is the Seebeck coefficient, R_M is module active resistance, Θ_M is hot-to-cold sides thermal resistance. TEM effectively drains up to 3-4W of heat from the cold side with an acceptable level of dissipation on the hot side, but its losses rise fast with the module's current and decrease the efficiency of the cooling.

A) Insulation cooling system

The first method uses a copper housing (envelope) to isolate the sensor from high ambient temperature and create acceptable environmental conditions inside the housing. The main target is to keep the temperature of the copper case below 85 ºC maintaining maximum acceptable operating temperature. In this case, temperatures of inner devices are not crucial parameters, as the manufacturer guarantees the operability. The appearance of the design and thermal model of the whole assembling are presented in Figure 133. TEM is attached to the surface of the housing by some TIM on the front face in the middle.

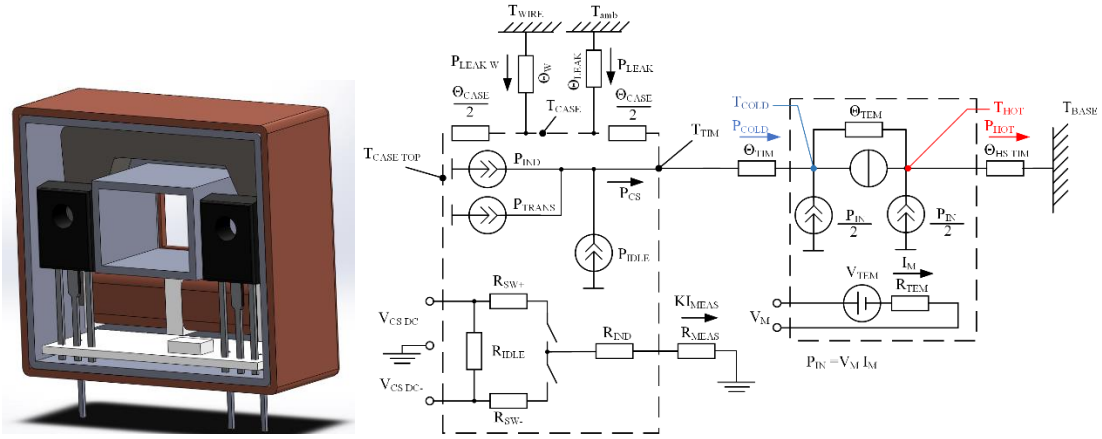


Figure 133 – Section of the proposed envelope design and a thermal model of the assemblance.

The heat leakage P_{LEAK} represents the amount of heat absorbed by the copper case from the environment due to temperature difference ($T_{AMB} - T_{CASE}$). Thermal resistance $\Theta_{CS\ LEAK}$ between the housing and air is calculated through the area of the housing (A_{CS}), heat exchange coefficient ($h_C = 5 \div 10 \frac{W}{m^2 K}$ for still air and natural convection, and up to 100 for forced airflow):

$$\Theta_{CS\,LEAK} = \frac{1}{h_C A_{CS}} \tag{64}$$

$$P_{LEAK} = h_C A_{CS}(T_{AMB} - T_{CASE}) \tag{65}$$

Extra thermal resistance (Θ_{CASE}) is added in series to account for heat transfer along the surface of the envelope towards the TEM. As P_{LEAK} depends on T_{CASE}, value of P_{COLD} also depends on T_{CASE}. To account for this dependency in the model, the equation for P_{COLD} includes Θ_{LEAK}, Θ_{CASE}, Θ_{TIM}, and T_{AMB}:

$$P_{COLD} = \frac{(P_{CS} + P_{LEAK\,W})\left(\Theta_{LEAK} + \frac{\Theta_{CASE}}{2}\right) + T_{AMB} - T_{COLD}}{\Theta_{LEAK} + \frac{\Theta_{CASE}}{2} + \Theta_{TIM}} \tag{66}$$

Generally, the primary current conductor has a higher temperature than the ambient due to self-heating by conductive losses. Therefore, an additional source of heat $P_{LEAK\,W}$ is required to account for extra heat transfer through the cable opening of the CS. The influence of that source is considered a constant power source for given I_{MEAS}. The actual value of power is evaluated during the experiment through temperature rise on the cold side when the CS is off.

Simulation results are presented in Figure 134, and show that this cooling extends the operating temperature range up to 120ºC of T_{BASE} (and T_{AMB} =140 ºC) with TEM consuming about 10W at the peak point. Beyond this point, TEM cannot maintain the temperature of CS below 85 ºC due to high T_{HOT}. At the target coolant temperature of 105 ºC, the minimum required V_m is about 2V, and minimum achievable temperature is about 72 ºC ($V_m = 3.5V$).

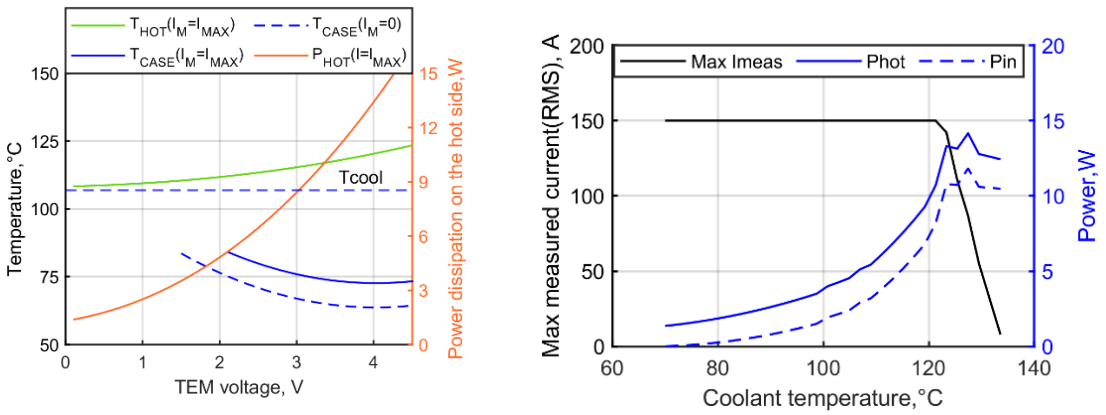


Figure 134 – Theoretical performance of the current sensor with cooling at different coolant temperature ($T_{AMB} = T_{COOL} + 20$°C, $h_C = 10\,\frac{W}{m^2K}$, $\theta_{Leak} = 43\,\frac{K}{W}$)

Experimental high-temperature testing is performed to evaluate the accuracy of the

thermal model and the calculation method. A current sensor installed inside a copper envelope and attached TEM are placed on a bulk aluminium plate (base) to absorb generated heat without significantly increasing the base temperature (T_{BASE}). A high-temperature drying oven heats up the whole structure to 105 ºC. Due to the nature of the oven, the air moves inside its inner volume, so convection is considered forced with high heat exchange between the sensor's cooling system and the environment. The average leakage thermal resistance at the start of testing is about 5.8 $\frac{K}{W}$ (heat exchange coefficient is about 75 $\frac{W}{m^2K}$). The experiment includes a number of stages to help assess the cooling performance in different operating conditions. During stages from 1 to 7 the sensor and current power supply are off, and power drained from the cold side is only leakage heat due to heat exchange. Module input voltage changes from 0.5V to 2.7V. At the 7th stage airflow configuration is different ($\Theta_{CS\ LEAK}$ increases from 5.8 $\frac{K}{W}$ to 4.8 $\frac{K}{W}$). The 8th stage is necessary to account for extra heat that is radiated by the power cable when the measured current is applied (the half of rated current). The 9th stage includes TEM and current sensor operation only (measured current is off) to evaluate quiescent current and related power losses. During the 10th stage normal operation of the sensor is observed (the half of rated current). EM input voltage has stayed the same since the 7th stage. Temperature probes are located on the hot side of TEM (T_{HOT}), the bottom of the copper envelope (just next to TEM's cold side, T_{CASE}) and in the air next to the sensor (T_{AIR}). Temperature measurements are presented in Figure 135. Hot side, cold side, and input powers are obtained by temperature values T_{HOT}, T_{CASE} and values for module input current I_M, V_M. According to the results, the heat leakage power P_{LEAK} dominates over all other sources even during the normal operation cycle.

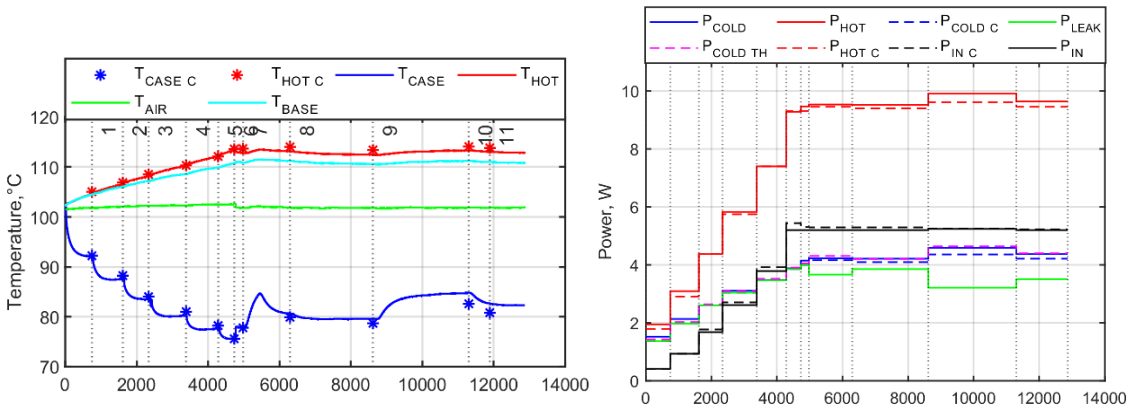


Figure 135 – Temperature measurements and power estimations for high temperature testing.

Base and ambient temperatures (T_{BASE}, T_{AMB}), module input voltage V_M, and specific parameters from experimental measurements (θ_{Leak}) are used to calculate case temperature $T_{CASE\ C}$ through equations of the thermal model. The error between measured values and the calculated one does not exceed 2-3 ºC. Results for hot side and cold side powers ($P_{HOT\ C}$, $P_{COLD\ C}$) and input power ($P_{IN\ C}$) almost match values that are obtained through measured temperatures T_{HOT}, T_{CASE}. Therefore, the thermal model could be used to predict the temperature of a current sensor with envelop cooling, estimate the required input DC power and dissipation power on the hot side. Temperature characteristics and power dissipation with the modified thermal resistance and experimentally measured heat transfer coefficient at different module input voltage are shown in Figure 136. Significantly higher heat exchange between the copper envelope and the environment in the experiment is responsible for higher minimal input voltage that is required to maintain sensor's temperature.

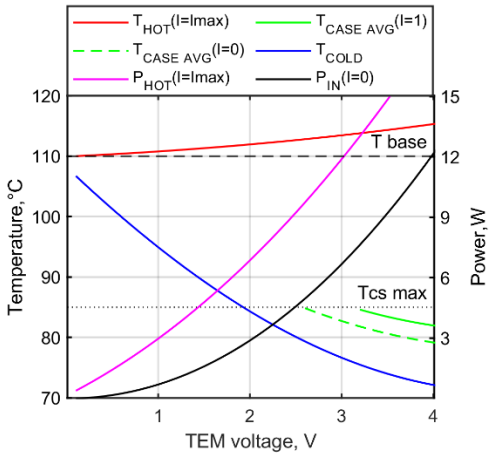


Figure 136 – Hot side and case temperatures and required input power at different TEM input voltage ($T_{BASE} = 110$℃, $T_{AMB} = 105$℃, $h_C = 73\frac{W}{m^2K}$, $\theta_{Leak} = 5.8\frac{K}{W}$).

The maximum measured current for two different values of the heat exchange coefficient is calculated and plots are shown in Figure 137. This design requires improved thermal insulation between the envelope and the environment because at high ambient temperature significant area of the housing heats up excessively and overloads the TEM.

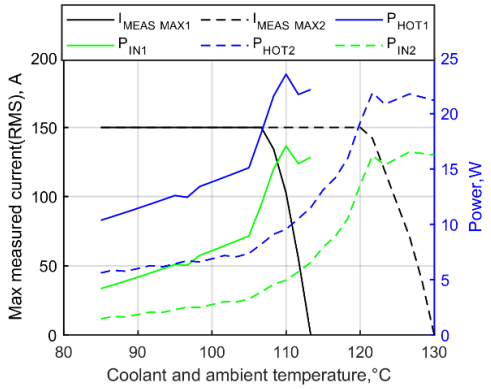


Figure 137 – Maximum measured current, required input DC power, and hot side power at different coolant (base) temperature ($\theta_{LEAK1} = 0.5\theta_{LEAK2}$)

Advantage of the method is the extension of operating conditions without modification of CS.

B) Cooling system with a heat sink.

The second method implies deeper modification of CS by adapting a heat sink made out of a copper plate (see Figure 138). The hottest elements are transistors and the coil. Less important is to cool the operational amplifier as its power consumption is relatively low and it could be replaced with the high temperature analogue without reduction in accuracy. Although coil cooling is not an ordinary task, it could be performed with a thermal grease or a thermal pad. Transistors are also connected to the heat sink through an electrically isolated TIM.

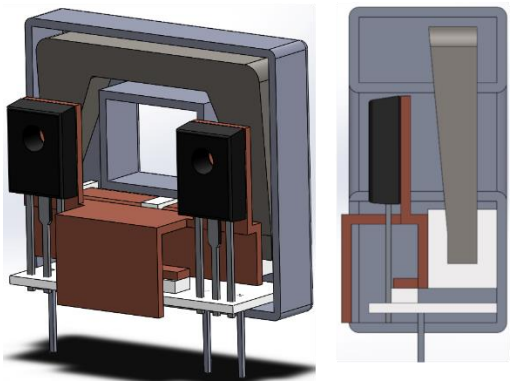


Figure 138 – Appearance of CS with a heat sink (HtS).

The proposed thermal model of modified CS is presented in Figure 139. Additional thermal resistances ($\theta_{IND\,HS}$, $\theta_{J\,HS}$) are placed between HtS, inductor, and transistor to represent thermal resistance of additional parts of HtS, TIM of inductor cooling, and heat exchange inside the CS by contrast with envelope cooling where all inner processes are not

considered. Values of leakage heat exchange primary wire $P_{LEAK\,W}$ is measured experimentally and used later in thermal model calculation.

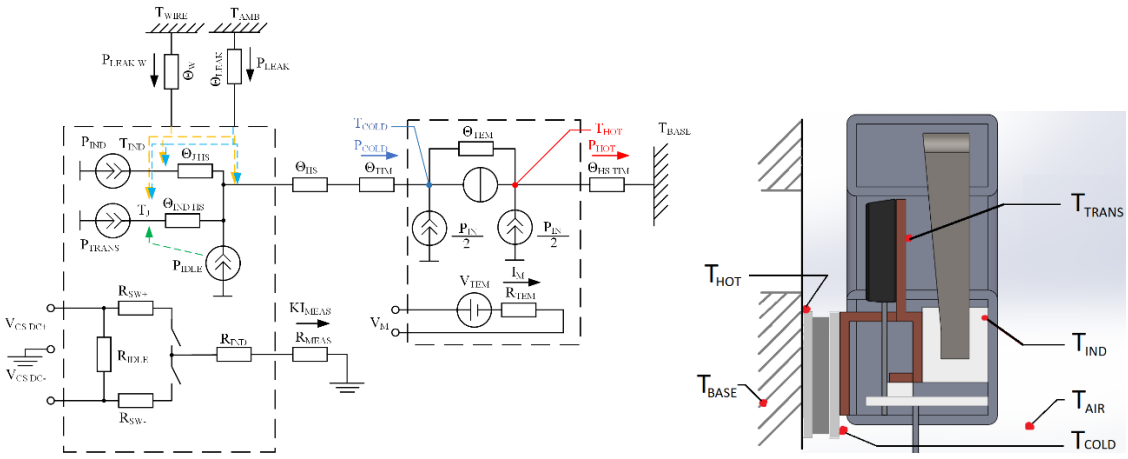


Figure 139 – Thermal model of CS with a heat sink and locations of temperature probes during the experiment.

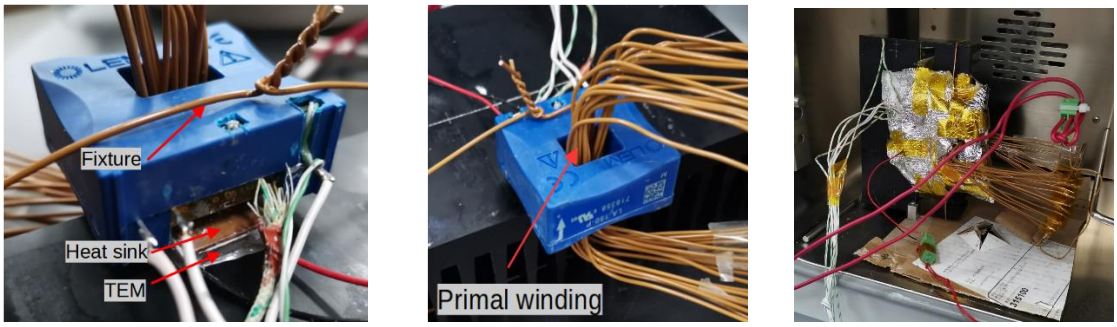


Figure 140 – CS with primary winding installed and CS with a thermal cover inside the chamber.

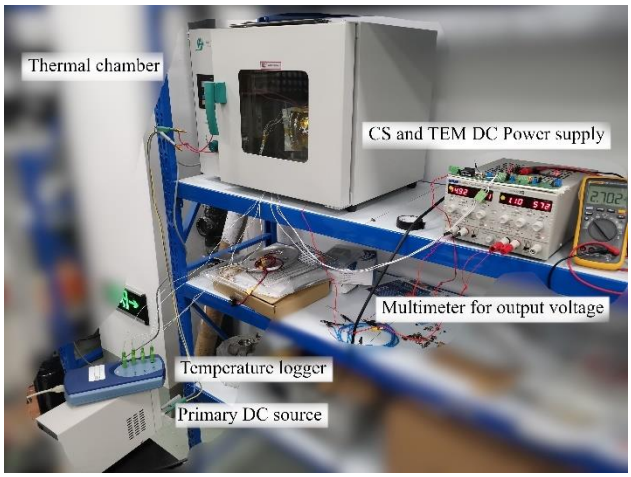


Figure 141 – Overview of the testing system.

In this design heat leakage P_{LEAK} is distributed between HtS (coldest part), transistors, PCB, and the coil with a core. For simplicity of calculation and the model, the value is linked to temperature difference ($T_{AMB} - T_{HtS}$).

$$P_{LEAK} = \frac{(T_{AMB} - T_{HtS})}{\theta_{LEAK\ EXP}} \quad (67)$$

As P_{LEAK} depends on T_{HtS}, value of P_{COLD} also depends on T_{HtS}. To account for this dependency into the model, the equation for P_{COLD} includes Θ_{LEAK}, Θ_{HtS}, Θ_{TIM}, and T_{AMB}:

$$P_{COLD} = \frac{(P_{CS} + P_{LEAK\,W})\Theta_{LEAK} + T_{AMB} - T_{COLD}}{\Theta_{LEAK} + \Theta_{HtS} + \Theta_{TIM}} \quad (68)$$

The experiment includes several stages with different operation modes to measure the impact of different factors (leakage, inner power dissipation, etc.) independently. The prepared CS and testing system are presented in Figure 140 and Figure 141. All tests are conducted with DC measured current at the maximum equivalent amplitude of 144 A (CS output current is 75 mA, measuring resistance is 37.5 Ohms), hence measuring DC is the most power consuming operation mode of CS. CS and primary circuit are off during the first and second operation stages (stages have different P_{IN}), and exchange with the environment can be evaluated. At the beginning of the 3rd stage CS is switched on ($P_{CS} = P_{IDLE}$), so P_{COLD} also includes P_{IDLE} this period. Then measured current is turned on for rest of testing time (maximum current for 4-6 periods and half of that value for 7-8 periods), and CS is off to measure $P_{LEAK\,W}$. The 5th stage is the normal operation of CS with maximum output current ($P_{CS} = P_{IDLE} + P_{IND\,MAX} + P_{TRANS\,MAX}$). The primary current changes direction for 6th period (the second transistor dissipates all transistors' losses), but P_{COLD} stays the same. During the 7th period, CS works in normal operation mode and measures half of maximum current ($P_{CS} = P_{IDLE} + 0.25P_{IND\,MAX} + 0.75P_{TRANS\,MAX}$, $P_{LEAK\,W} \approx 0.25P_{LEAK\,W\,MAX}$). CS is switched off for 8th period, and measured current is a half of its maximum value.

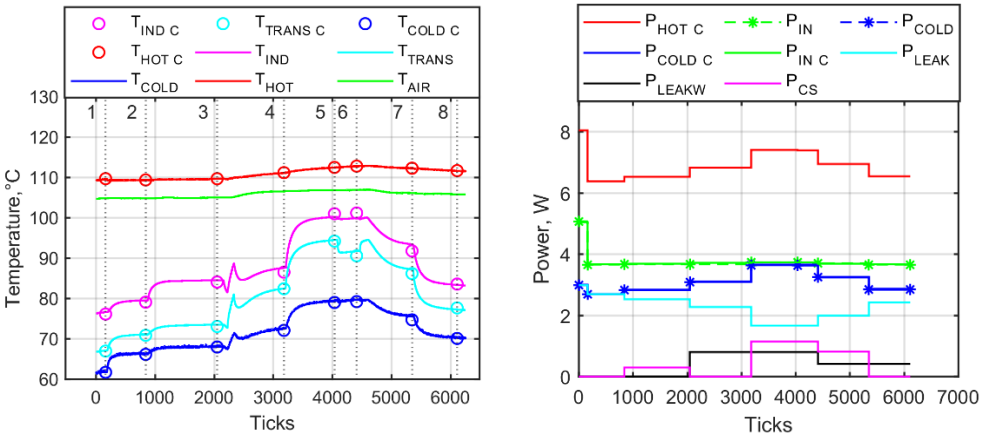


Figure 142 – Test results of CS with a heat sink.

Test results are presented in Figure 142. Values indicated with round markers ($T_{IND\,C}$, $T_{TRANS\,C}$, $T_{COLD\,C}$, $T_{HOT\,C}$) are values that are obtained with thermal model calculations by

the base and ambient temperatures (T_{BASE}, T_{AMB}), module input voltage V_M, and specific parameters from experimental measurements ($P_{LEAK\,W}$, θ_{LEAK}). The tested CS is exposed to the same air conditions (the same temperature chamber, no cover) as the previous one. However, the heat exchange with ambient is significantly lower ($\theta_{Leak\,HtS} = 12.5\,\frac{K}{W}$ against $\theta_{Leak\,CU} = 5.8\,\frac{K}{W}$) due to embedded structure of cooling element, smaller area of cold elements and higher temperature of cooling. Therefore P_{LEAK} is less almost by 40%.

Due to complex thermal interaction between different parts of the sensor, several modifications must be performed with the thermal model:

$$T_{TRANS} = (P_{TRANS} + x_1 P_{IDLE} + y_1 P_{LEAK\,W})\Theta_{TR\,HtS} + P_{COLD}\,(\Theta_{HtS}+\Theta_{TIM}) + T_{COLD} \quad (69)$$

$$T_{IND} = (P_{IND} + x_2 P_{IDLE} + y_2 P_{LEAK\,W} + z_2 P_{LEAK})\Theta_{IND\,HtS} + P_{COLD}\,(\Theta_{HtS}+\Theta_{TIM}) + T_{COLD} \quad (70)$$

$$P_{COLD} = P_{TRANS} + P_{IND} + P_{IDLE} + P_{LEAK} + P_{LEAK\,W} \quad (71)$$

where $x_{1,2}$, $y_{1,2}$, z_2 – scale coefficients that represent influence of heat exchange inside CS (values are stated in TABLE 30).

Table 30 - Scale coefficients of modified thermal model

Coefficient	Value	Thermal resistance	Value
x_1	0.05	$\Theta_{TR\,HtS}$	5
y_1	0.85	$\Theta_{IND\,HtS}$	16
x_2	0.7	Θ_{HS}	1.75
y_2	0.15	Θ_{TIM}	0.3
z_2	0.2		

Coefficients reflect the physical structure of CS and highly rely on distances from components to heat sources. Transistors' cases are very close to the walls of primary conductor's pass, therefore a significant amount of heat generated by primary current is being absorbed by transistors. By contrast, the coil and a sensor's core have a larger gap and are less sensitive to that heat source. On the other hand, P_{IDLE} is generated mostly by current limiting resistors which are located just under the coil; thus, the correlated coefficient is higher for the coil temperature.

Considering the base temperature as constant and using other parameters from the experiment results the temperature-volts characteristic could be obtained with thermal model simulation (results in Figure 143).

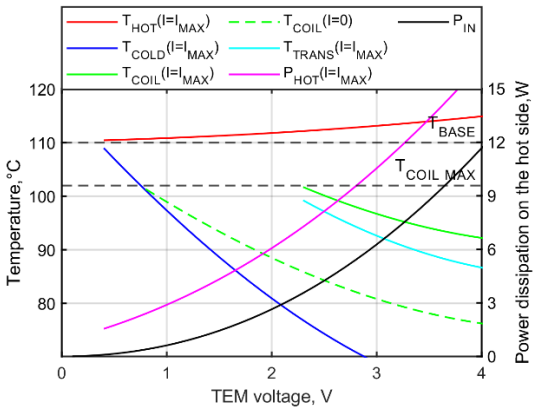


Figure 143 – Key temperatures of HtS CS and required input power at different TEM input voltage ($T_{BASE} = 110℃$, $T_{AMB} = 105℃$, $\theta_{Leak} = 12.5\frac{K}{W}$).

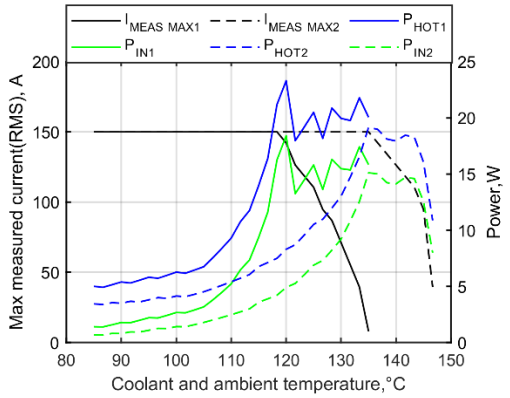


Figure 144 - Maximum measured current, required input DC power, and hot side power at different coolant (base) temperature ($\theta_{LEAK1} = 0.5\theta_{LEAK2}$)

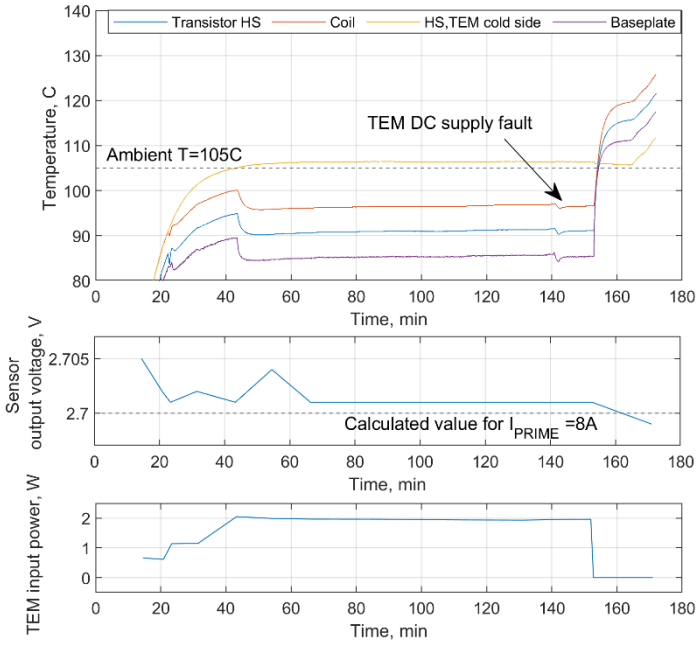


Figure 145 – Long term operation of the sensor with HS modification.

Comparison between two designs shows that HS cooling is more effective extending operating temperature region by 10-15℃ in high temperature operations (see Figure 144).

In Figure 145 CS operates for almost 2 hours under ambient temperature of 105 ºC without significant change in its output voltage. Total input current of 144A on primary side is formed by 18 loops with 8A DC current in each loop. At 152 minute TEM is switched off, and ambient temperature is increased to 115 ºC to create stress conditions for CS. Although coil temperature exceeds rating temperature of coil's Hall sensor by more than 10 ºC, measurements are correct, and no fail detected.

5.4 Power supply and control for HS cooling system

Both proposed cooling designs require an external power supply to provide the correct DC voltage V_M for cooling operation. The efficiency of the TEM rapidly drops with voltage above 3-3.5V due to the non-linear characteristics of active losses inside the module. Power supply with fixed voltage is a feasible and simple solution, but it does not provide flexibility regarding operation temperature. TEM can cool down CS to a negative temperature in case of normal ambient temperature and high V_M. Moreover, power losses could be excessively high when the system does not need cooling at all. Variable voltage sources with such a low output voltage and high current are not typical for power electronics systems, as usually operating voltage starts with fixed 3.3V or 5V and higher.

An embedded automatic system with close-loop temperature control and temperature sensor can regulate dissipating power when necessary. Developing a high-temperature DC/DC converter with high output current is challenging and decreasing operating conditions might greatly reduce design complexity. Therefore, it is worthwhile to consider if TEM is able to cool both CS and DC/DC converter. Assuming the typical efficiency η of DC/DC converters at 0.8, the equation for the power of the cold side could be modified as follows:

$$\mathrm{P}_{COLD} = \frac{(P_{CS} + P_{LEAK\,W})\Theta_Y + T_{AMB} - T_{COLD}}{\Theta_Y + \Theta_X} + (1-\eta)V_M I_M \qquad (72)$$

where Θ_X, Θ_Y are specific thermal resistances (according to thermal models). Leakage losses of DC/DC converter and the possible increase in contact thermal resistance with TEM are not considered here. Results of simulation for both types of cooling systems are presented in Figure 146. Simulation is performed with parameters calculated by experiment, and minimal T_{AMB} is 105 ºC. Additional power losses on the cold side significantly reduce operating temperature in case of high heat leakage, and usage of

envelope cooling system becomes not reasonable without thermal insulation measures.

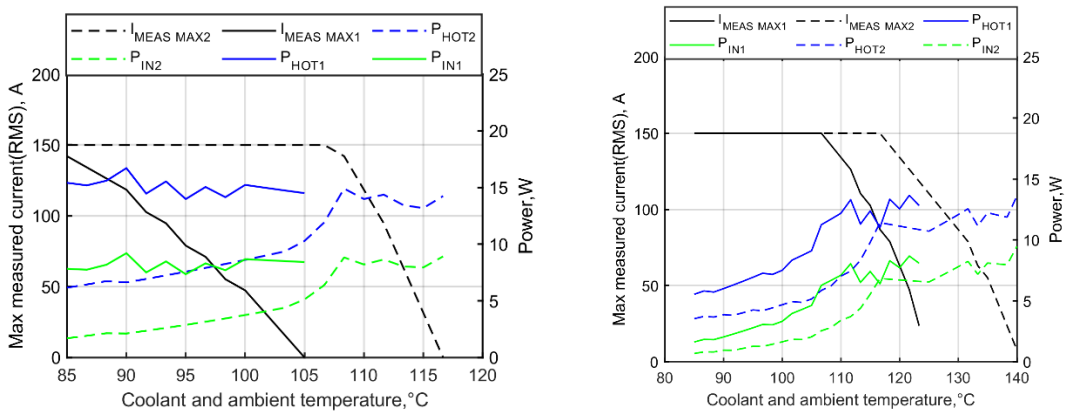


Figure 146 - Maximum measured current, required input DC power, and hot side power at different base temperature (left – envelope cooling, right – HS design)

The block scheme of the proposed temperature controller includes a temperature sensor, an amplifier, variable resistance, and a controlled buck converter (see Figure 147).

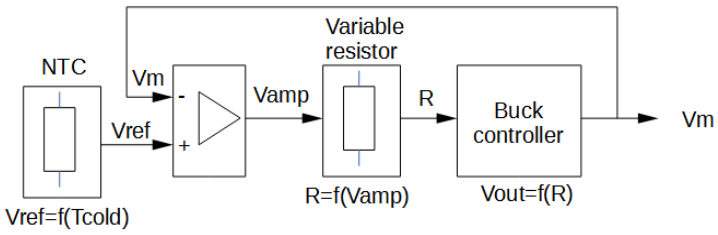


Figure 147 – Block scheme of the automatic temperature controller.

Temperature sensor based on NTC sensor generates voltage V_{REF} according to required temperature-volts characteristic; its output voltage acts as a reference voltage for an amplifier that regulates the output voltage of DC/DC converter through variable resistance circuit. Correlations between temperature, NTC resistance and the reference voltage of DC/DC controller are shown in Figure 148.

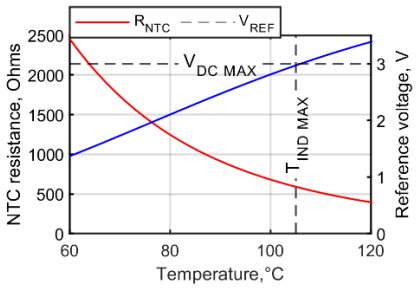


Figure 148 – Resistance curve of NTC resistor and reference voltage at different temperatures.

The circuit includes a parallel connection of resistor and MOSFET with high $R_{DS\,ON}$ controlled by the operational amplifier. At the same time, the circuit is a part of DC/DC converter's close-loop control circuit, therefore the change in resistance value causes

altering in output voltage. The concept design of such an automatic temperature controller and a view of the assembled cooling system are presented in Figure 149.

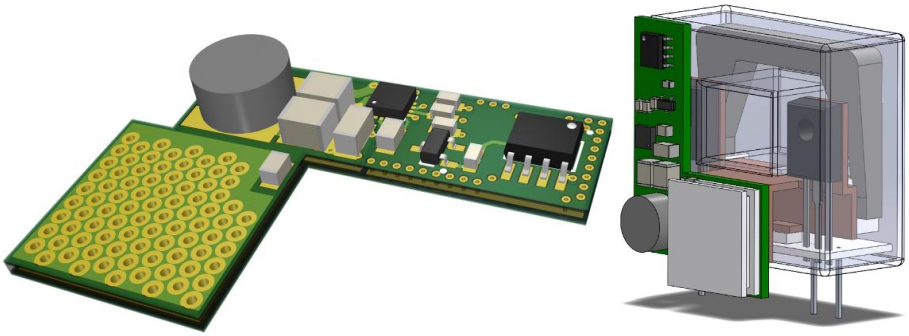


Figure 149 – Appearance of DC/DC-converter and its position on the current sensor.

A simplified version of the embedded power source for cooling (in case of stable ambient temperature) can operate with threshold control (not continues) and trigger the TEM when the temperature is higher than the specified value.

This modification shows that it is possible to extend the temperature range of industrial close-loop CS with the help of TEM.

5.5 Chapter summary

The chapter presents methods to increase the operating temperature range of closed loop current sensor LA-150P using TEM. The inner structure of the sensor is explained with the most heat-generating parts highlighted. Thermal models with related equation systems are created for the unmodified sensor and both modifications, including TEM thermal model. Experimental results fit the theoretical expectations of inner temperature under different operation conditions. Both methods can enlarge the sensor's temperature range by at least 30°C if proper thermal insulation is applied to prevent heat leakages. At the same time, the most promising method (with an inner heatsink) requires additional investigation regarding reliability issues and is more suitable as a concept for further industrial research. TEM also demands a significant amount of input power to maintain a large temperature difference that, in most cases, would require an external low-voltage power supply.

Chapter 6

6 Conclusion

6.1 Main Contributions

This thesis studies the design procedures of the integrated inverters with motors. Special focus is made on operations under high ambient/coolant temperatures.

In Chapter 2 possible IMD classifications and cooling techniques including thermal stacks for different packages and coldplate designs are reviewed. Analysis of 38 IMDs and 13 HT inverters at different stages of maturity (theoretical model, prototype or commercial sample) shows the rapid development of integration technology and increasing interest in high power IMD (both for normal and high operating temperatures) from industry and academia. At the same time, it is revealed only limited variety of power semiconductors's types and cooling techniques is used in such applications. The power modules dominate all other devices due to the simplicity of the overall design process at the expense of package unification and freedom in component selection. Moreover, capabilities of PE with paralleled discrete components are not well studied in case of IMD application. Detailed parametric model of such PE, which include several crucial parameters for volumetric and thermal analysis, is proposed to address this question and described in the next chapters.

The component database including SMT SiC MOSFETs (21 types), THT SiC MOSFETs (9 types), and power modules (10 types) is collected for further comparison analysis. Two operation modes, i.e. given output power with determined V_{DC} and maximum output power with optional V_{DC}, are used for better demonstration. In low-power applications (up to 50kW), both SMT and THT discrete devices show the same performance as power modules have. However, THT devices and power modules only would be the preferable choice for high power applications. For HT applications, restrictions on the case temperature of power modules noticeably limit maximum coolant temperature and maximum output power, and discrete elements do not have such restrictions. As expected, the most recent types show significant improvement in thermal performance and output power by comparison with old ones within the same package and dimensions. That shows that inverter performance could be improved merely by replacement of older devices with the new ones without modifications of layout, PCB structure etc.

Differences in MOSFET characteristics could significantly affect the thermal conditions

of devices if left unaddressed or without proper attention. Two major factors of output power derating, i.e., the unequal threshold voltage and different on-state channel resistance, are evaluated, and the required value of the derating is shown. The positive temperature coefficient of channel resistance that acts as a compensatory mechanism helps prevent thermal runaway of the overheated MOSFET, but it has limited effect to equalize junction temperatures of parallel devices. Component selection is the most effective way to eliminate the difference in characteristics and reach the highest figures in output power without serious increase in the number of components and circuit complexity.

The thermal model complemented by the dataset of 30kW PMSM and the cold plate model is used to calculate the power densities of the complete IMD with various types of SMT MOSFETs. The square shape of inverter shows a higher density of MOSFET layout than the round one; therefore, it is the preferable choice if the system structure does not apply other restrictions (e.g., shaft extension, encoder presence, etc.). For given power level, machines' characteristics, and IMD structure the maximum achievable values of gravimetric and volumetric power densities are 6 kW/kg and 16 kW/L. PE mainly contributes to the volume of IMD occupying 50-75% of total space, and MOSFET characteristics significantly affect the performance and dimensions of the inverter.

Volumetric characteristics of DC-link capacitor bank for HT application are evaluated in the thesis as it usually occupies a significant amount of IMD's inner space. According to the results, the highest density is achieved with modern PLZT capacitors, although a great quantity of capacitors is required to achieve required capacitance. The price factor might be significant in real applications and prevent the usage of these capacitors in large numbers. Evaluation of PCB quantity for each type of capacitor shows that for typical low and middle power applications, a single square PCB of about 200cm^2 can accommodate the necessary number of capacitors if $F_{SW} > 50kHz$. Low switching frequency or high phase current lead to a substantial increase in minimum DC-link capacitance.

Crosstalk issue caused by fast MOSFET switching process is discussed in Chapter 4 with a focus on operations of paralleled MOSFETs. The results of the simulations could be summarized as follows:

- with small switching time, high Vdc, and high temperature, the negative effect of crosstalk could become noticeable (especially for devices with low threshold voltage V_{TH}), leading to an increase in switching power losses and additional self-heating of MOSFETs.

- Additional parasitic inductance has a limited effect on the amplitude of crosstalk voltage in the range of 10-100 nH, therefore, all paralleled MOSFETs experience almost the same level of injected current and induced gate voltage regardless of their position in the group.
- Lower external gate resistance does not help to “remove” injected current from the gate but increases it due to a faster transition of drain voltage.
- Crosstalk voltage cannot be eliminated entirely due to the existence of inner parasitic elements in the gate circuit of MOSFET. The parasitic voltage is generated on the gate even with short-circuit between the gate pins. Therefore, the shift of gate voltage to the negative area is required to guarantee “open” status during the turn-off period.

The proposed modification of GD offers a reduction of crosstalk voltage for both polarities without a significant increase in gate driver power. The circuit also does not occupy much PCB space and does not require wide traces for operation as the high current circulates in the vicinity of the gate. For the given MOSFET and gate structure the crosstalk reduction is about 1V.

Chapter 5 presents the study on methods to increase the operating temperature range of closed loop current sensor LA-150P using TEM. Both methods can enlarge the sensor's temperature range by at least 30°C if proper thermal insulation is applied to prevent heat leakages. At the same time, the most promising method (with inner heatsink) requires additional investigation regarding reliability issues and is more suitable as a concept for further industrial research. TEM also demands a significant amount of input power to maintain a large temperature difference that, in most cases, would require an external low voltage power supply.

6.2 Future research

Future studies that extend and supplement the research of this thesis include the following topics:

1. Usage of discrete MOSFET in IMD implementation with deep integration of PE and EM (inner location of PE or even its direct attachment to the stator core) might be beneficial for power density due to the small package height. Design of such IMD can push further the limits for output power and density of IMD with inner PE.

2. Design of high power full SiC IMD with very high switching frequency and focusing on minimization of DC-link capacitor and filters to increase power density and reduce overall dimensions. Low switching losses for some SiC MOSFETs let them operate at high switching frequency without significantly reducing inverter efficiency.
3. Reduction of space between parallel power switches or stacked layout can increase space utilization. However, too tight layout causes mutual heating. Double-sided cooling can increase heat transfer area and be suitable for the stacked structure. Today only custom design power modules use this technology, but they are unavailable for most customers. Inverter design using half-bridge or 3-phase power devices with parallel discrete MOSFETs might be an interesting solution.

References

[1] K. Hayhoe, D.J. Wuebbles, D.R. Easterling, D.W. Fahey, S. Doherty, J. Kossin, W. Sweet, R. Vose, and M. Wehner, Ed. *2018: Our Changing Climate* (Impacts, Risks, and Adaptation in the United States: Fourth National Climate Assessment. Washington, DC, USA: U.S. Global Change Research Program, 2018, pp. 72–144.

[2] IEA, "Greenhouse Gas Emissions from Energy: Overview," IEA, Paris, 2021. [Online]. Available: https://www.iea.org/reports/greenhouse-gas-emissions-from-energy-overview

[3] "Determining the environmental impacts of conventional and alternatively fuelled vehicles through LCA," European Commission, 2020. [Online]. Available: https://ec.europa.eu/clima/document/download/799b37ba-7d91-484a-97e2-f0cb36dd57f0_en

[4] M. R. Hannah Ritchie, Pablo Rosado, "CO_2 and Greenhouse Gas Emissions," *Our World in Data,* 2020. [Online]. Available: https://ourworldindata.org/co2-and-other-greenhouse-gas-emissions.

[5] C. McKerracher *et al.*, "Electric vehicle outlook 2020," *Bloomberg New Energy Finance,* 2020.

[6] I. E. Agency. "Electric and plug-in hybrid vehicle roadmap." https://iea.blob.core.windows.net/assets/91a4a053-8738-4bf2-895e-f4213a4a1253/EV_PHEV_brochure.pdf (accessed.

[7] H.-C. Liu, X.-Y. You, Y.-X. Xue, and X. Luan, "Exploring critical factors influencing the diffusion of electric vehicles in China: A multi-stakeholder perspective," *Research in Transportation Economics,* vol. 66, pp. 46-58, 2017/12/01/ 2017, doi: https://doi.org/10.1016/j.retrec.2017.10.001.

[8] G. Conway, A. Joshi, F. Leach, A. García, and P. K. Senecal, "A review of current and future powertrain technologies and trends in 2020," *Transportation Engineering,* vol. 5, p. 100080, 2021/09/01/ 2021, doi: https://doi.org/10.1016/j.treng.2021.100080.

[9] Nissan. "In-wheel motor." https://www.nissan-global.com/EN/TECHNOLOGY/OVERVIEW/in_wheel_motor.html (accessed.

[10] K. Akatsu and S. Tanimoto, "Air-Cooled Multi-Phase Dual-Winding In-Wheel Motor Integrated with Ultra Small SiC Module," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 11-15 Oct. 2020 2020, pp. 41-46, doi: 10.1109/ECCE44975.2020.9236414.

[11] IATA, "Aircraft Technology Roadmap to 2050." [Online]. Available: https://www.iata.org/en/programs/environment/technology-roadmap/

[12] P. Wheeler and S. Bozhko, "The More Electric Aircraft: Technology and challenges," *IEEE Electrification Magazine,* vol. 2, no. 4, pp. 6-12, 2014, doi: 10.1109/MELE.2014.2360720.

[13] W. Lee, S. Li, D. Han, B. Sarlioglu, T. A. Minav, and M. Pietola, "Achieving high-performance electrified actuation system with integrated motor drive and wide bandgap power electronics," in *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, 11-14 Sept. 2017 2017, pp. P.1-P.10, doi: 10.23919/EPE17ECCEEurope.2017.8099359.

[14] H. Shimizu, T. Okubo, I. Hirano, S. Ishikawa, and M. Abe, "Development of an Integrated Electrified Powertrain for a Newly Developed Electric Vehicle," 2013. [Online]. Available: https://doi.org/10.4271/2013-01-1759.

[15] "GM provides technical details of the Gen 2 Voltec propulsion system used in the 2016 Volt." https://www.greencarcongress.com/2015/04/20150423-voltec.html (accessed.

[16] "Power electronics. Industry Challenges 2020-2035+." https://www.apcuk.co.uk/app/uploads/2021/09/https___www.apcuk_.co_.uk_app_uploads_2021_05_https___www.apcuk_.co_.uk_app_uploads_2021_05_Industry-Challenge-

Report-Power-Electronics.pdf (accessed.
[17] D. Bergogne *et al.*, "Towards an airborne high temperature SiC inverter," in *2008 IEEE Power Electronics Specialists Conference*, 15-19 June 2008 2008, pp. 3178-3183, doi: 10.1109/PESC.2008.4592442.
[18] R. W. Johnson, J. L. Evans, P. Jacobsen, J. R. Thompson, and M. Christopher, "The changing automotive environment: high-temperature electronics," *IEEE Transactions on Electronics Packaging Manufacturing,* vol. 27, no. 3, pp. 164-176, 2004, doi: 10.1109/TEPM.2004.843109.
[19] B. Wrzecionko, D. Bortis, and J. W. Kolar, "A 120 °C Ambient Temperature Forced Air-Cooled Normally-off SiC JFET Automotive Inverter System," *IEEE Transactions on Power Electronics,* vol. 29, no. 5, pp. 2345-2358, 2014, doi: 10.1109/TPEL.2013.2294906.
[20] T. Funaki *et al.*, "Power Conversion With SiC Devices at Extremely High Ambient Temperatures," *IEEE Transactions on Power Electronics,* vol. 22, no. 4, pp. 1321-1329, 2007, doi: 10.1109/TPEL.2007.900561.
[21] T. M. Jahns and H. Dai, "The past, present, and future of power electronics integration technology in motor drives," *CPSS Transactions on Power Electronics and Applications,* vol. 2, no. 3, pp. 197-216, 2017, doi: 10.24295/CPSSTPEA.2017.00019.
[22] J. Wang, Y. Li, and Y. Han, "Evaluation and design for an integrated modular motor drive (IMMD) with GaN devices," in *2013 IEEE Energy Conversion Congress and Exposition*, 15-19 Sept. 2013 2013, pp. 4318-4325, doi: 10.1109/ECCE.2013.6647278.
[23] T. M. Jahns and B. Sarlioglu, "The Incredible Shrinking Motor Drive: Accelerating the Transition to Integrated Motor Drives," *IEEE Power Electronics Magazine,* vol. 7, no. 3, pp. 18-27, 2020, doi: 10.1109/MPEL.2020.3011275.
[24] A. Shea and T. M. Jahns, "Hardware integration for an integrated modular motor drive including distributed control," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 14-18 Sept. 2014 2014, pp. 4881-4887, doi: 10.1109/ECCE.2014.6954070.
[25] P. W. Wheeler *et al.*, "A fully integrated 30 kW motor drive using matrix converter technology," in *2005 European Conference on Power Electronics and Applications*, 11-14 Sept. 2005 2005, pp. 9 pp.-P.9, doi: 10.1109/EPE.2005.219268.
[26] M. Maerz, M. H. Poech, E. Schimanek, and A. Schletz, "Mechatronic integration into the hybrid powertrain–the thermal challenge," 2006 2006, pp. 1-6.
[27] M. D. P. Emilio. "SiC Challenges for Power Electronics." https://www.powerelectronicsnews.com/sic-vendors-tackle-production-challenges-for-power-electronics/ (accessed.
[28] I. P. Ltd. "CTU400 Automotive EPS." https://integralp.com/communication/product/ctu400-automotive-eps/#edd-free-download-modal (accessed.
[29] I. P. Ltd. "IPM 278 LV Platform." https://integralp.com/communication/product/ipm-278-lv-platform/ (accessed.
[30] N. Group. "EV Traction Motor System E-Axle." https://www.nidec.com/en/technology/new_field/e-axle/ (accessed.
[31] BorgWarner. "Product sheet. Integrated Drive Module (iDM) for Hybrid and Electric Vehicles." https://cdn.borgwarner.com/docs/default-source/default-document-library/integrated-drive-module-product-sheet.pdf?sfvrsn=7fda823c_14 (accessed.
[32] "HIGH VOLTAGE AXLE DRIVE (EMR3)." https://www.vitesco-technologies.com/en-us/products/high-voltage-axle-drive-(emr3) (accessed.
[33] Helix. "Integrated Drive Systems." https://ehelix.com/integrated-drive-systems/ (accessed.
[34] H3X. "H3X integrated motor drive for aircraft applications." https://www.h3x.tech/#amcoils (accessed.
[35] T. Friedli and J. W. Kolar, "A Semiconductor Area Based Assessment of AC Motor Drive Converter Topologies," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics*

Conference and Exposition, 15-19 Feb. 2009 2009, pp. 336-342, doi: 10.1109/APEC.2009.4802678.

[36] H. Beiranvand, E. Rokrok, and M. Liserre, "Volume Optimization in Si IGBT based Dual-Active-Bridge Converters," in *2019 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC)*, 12-14 Feb. 2019 2019, pp. 577-582, doi: 10.1109/PEDSTC.2019.8697785.

[37] B. Cheong, P. Giangrande, X. Zhang, M. Galea, P. Zanchetta, and P. Wheeler, "Evolutionary Multiobjective Optimization of a System-Level Motor Drive Design," *IEEE Transactions on Industry Applications,* vol. 56, no. 6, pp. 6904-6913, 2020, doi: 10.1109/TIA.2020.3016630.

[38] A. H. Mohamed, H. Vansompel, and P. Sergeant, "Electrothermal Design of a Discrete GaN-Based Converter for Integrated Modular Motor Drives," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 9, no. 5, pp. 5390-5406, 2021, doi: 10.1109/JESTPE.2021.3058107.

[39] S. Mohan. T. I. Incorporated. (2019). Thermal Comparison of FR-4 and Insulated Metal Substrate PCB for GaN Inverter. Available: https://www.ti.com/lit/an/tida030/tida030.pdf?ts=1647428129635&ref_url=https%253A%252F%252Fwww.google.com%252F

[40] M. Schiestl *et al.*, "Development of a High Power Density Drive System for Unmanned Aerial Vehicles," *IEEE Transactions on Power Electronics,* vol. 36, no. 3, pp. 3159-3171, 2021, doi: 10.1109/TPEL.2020.3013899.

[41] B. Mouawad, J. Espina, J. Li, L. Empringham, and C. M. Johnson, "Novel Silicon Carbide Integrated Power Module for EV application," in *2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, 16-18 May 2018 2018, pp. 176-180, doi: 10.1109/WiPDAAsia.2018.8734672.

[42] L. d. Lillo, B. Ahmadi, L. Empringham, M. Johnson, J. Espina, and R. Abebe, "Next Generation Integrated Drive, NGID: A Novel Approach to Thermal and Electrical Integration of High Power Density Drives in Automotive Applications," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 23-27 Sept. 2018 2018, pp. 1228-1232, doi: 10.1109/ECCE.2018.8558001.

[43] J. Wang, Y. Li, and Y. Han, "Integrated Modular Motor Drive Design With GaN Power FETs," *IEEE Transactions on Industry Applications,* vol. 51, no. 4, pp. 3198-3207, 2015.

[44] M. Horio, Y. Iizuka, and Y. Ikeda, "Packaging technologies for SiC power modules," *Fuji Electric Review,* vol. 58, no. 2, pp. 75-78, 2012.

[45] T. Ikeyama, K. Ishikawa, and N. Nozawa, "Development of power control unit for compact-class vehicle," SAE Technical Paper, 0148-7191, 2020.

[46] A. H. Mohamed, H. Vansompel, and P. Sergeant, "An Integrated Modular Motor Drive With Shared Cooling for Axial Flux Motor Drives," *IEEE Transactions on Industrial Electronics,* vol. 68, no. 11, pp. 10467-10476, 2021, doi: 10.1109/TIE.2020.3028818.

[47] M. Nikouie, H. Zhang, O. Wallmark, and H. Nee, "A highly integrated electric drive system for tomorrow's EVs and HEVs," in *2017 IEEE Southern Power Electronics Conference (SPEC)*, 4-7 Dec. 2017 2017, pp. 1-5, doi: 10.1109/SPEC.2017.8333555.

[48] X. Deng, S. Lambert, B. Mecrow, and M. A. S. Mohamed, "Design Consideration of a High-Speed Integrated Permanent Magnet Machine and its Drive System," in *2018 XIII International Conference on Electrical Machines (ICEM)*, 3-6 Sept. 2018 2018, pp. 1465-1470, doi: 10.1109/ICELMACH.2018.8507155.

[49] G. Su, L. Tang, C. Ayers, and R. Wiles, "An inverter packaging scheme for an integrated segmented traction drive system," in *2013 IEEE Energy Conversion Congress and Exposition*, 15-19 Sept. 2013 2013, pp. 2799-2804.

[50] A. Fuerback, T. Soeiro, M. Jacoboski, M. L. Heldwein, and A. Perin, "Integrated Motor Drive Design for an All-Electric Boat," 2014.

[51] "Tesla Model 3." Wikipedia. https://en.wikipedia.org/wiki/Tesla_Model_3#Engineering_and_changes (accessed.

[52] M. März, A. Schletz, B. Eckardt, S. Egelkraut, and H. Rauh, "Power electronics system integration for electric and hybrid vehicles," 2010 2010: IEEE, pp. 1-10.

[53] F. Hilpert, K. Brinkfeldt, and S. Arenz, "Modular integration of a 1200 v SiC inverter in a commercial vehicle wheel-hub drivetrain," in *2014 4th International Electric Drives Production Conference (EDPC)*, 30 Sept.-1 Oct. 2014 2014, pp. 1-8, doi: 10.1109/EDPC.2014.6984400.

[54] T. Burress, "Benchmarking EV and HEV technologies," *Oak Ridge National Laboratory,* 2016.

[55] M. Anwar, S. M. N. Hasan, M. Teimor, M. Korich, and M. B. Hayes, "Development of a power dense and environmentally robust traction power inverter for the second-generatio chevrolet VOLT extended-range EV," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 20-24 Sept. 2015 2015, pp. 6006-6013, doi: 10.1109/ECCE.2015.7310502.

[56] O. Kitazawa, T. Kikuchi, M. Nakashima, Y. Tomita, H. Kosugi, and T. Kaneko, "Development of power control unit for compact-class vehicle," *SAE International Journal of Alternative Powertrains,* vol. 5, no. 2, pp. 278-285, 2016.

[57] M. Anwar, M. Teimor, P. Savagian, R. Saito, and T. Matsuo, "Compact and high power inverter for the Cadillac CT6 rear wheel drive PHEV," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 18-22 Sept. 2016 2016, pp. 1-7, doi: 10.1109/ECCE.2016.7854931.

[58] J. Doerr, G. Fröhlich, A. Stroh, and M. Baur, "The Electric Drivetrain with Three-motor Layout of the Audi E-tron S," *MTZ worldwide,* vol. 81, no. 7, pp. 16-25, 2020/07/01 2020, doi: 10.1007/s38313-020-0254-2.

[59] A. Technologies. "Cold plates." https://www.amstechnologies-webshop.com/media/pdf/a8/8e/15/Cold-Plates-AMS-Technologies-Brochure.pdf (accessed.

[60] G. Mademlis, R. Orbay, Y. Liu, N. Sharma, R. Arvidsson, and T. Thiringer, "Multidisciplinary cooling design tool for electric vehicle SiC inverters utilizing transient 3D-CFD computations," *eTransportation,* vol. 7, p. 100092, 2021/02/01/ 2021, doi: https://doi.org/10.1016/j.etran.2020.100092.

[61] A. C. Iradukunda, D. R. Huitink, and F. Luo, "A Review of Advanced Thermal Management Solutions and the Implications for Integration in High-Voltage Packages," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 1, pp. 256-271, 2020, doi: 10.1109/JESTPE.2019.2953102.

[62] S. Jones-Jackson, R. Rodriguez, and A. Emadi, "Jet Impingement Cooling in Power Electronics for Electrified Automotive Transportation: Current Status and Future Trends," *IEEE Transactions on Power Electronics,* vol. 36, pp. 10420-10435, 2021.

[63] K. Oliphant, B. W. Webb, and M. Q. McQuay, "An experimental comparison of liquid jet array and spray impingement cooling in the non-boiling regime," *Experimental Thermal and Fluid Science,* vol. 18, no. 1, pp. 1-10, 1998/09/01/ 1998, doi: https://doi.org/10.1016/S0894-1777(98)10013-4.

[64] C. H. Hoang *et al.*, "A Review of Recent Developments in Pumped Two-Phase Cooling Technologies for Electronic Devices," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 11, no. 10, pp. 1565-1582, 2021, doi: 10.1109/TCPMT.2021.3117572.

[65] R. Xu, G. Wang, and P. Jiang, "Spray Cooling on Enhanced Surfaces: A Review of the Progress and Mechanisms," *Journal of Electronic Packaging,* vol. 144, no. 1, 2021, doi: 10.1115/1.4050046.

[66] A. Michalak *et al.*, "A Thermal Management Design Methodology for Advanced Power Electronics Utilizing Genetic Optimization and Additive Manufacturing Techniques," in *2020 19th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 21-23 July 2020 2020, pp. 547-557, doi:

10.1109/ITherm45881.2020.9190444.
[67] R. Khazaka, L. Mendizabal, D. Henry, and R. Hanna, "Survey of High-Temperature Reliability of Power Electronics Packaging Components," *IEEE Transactions on Power Electronics,* vol. 30, no. 5, pp. 2456-2464, 2015, doi: 10.1109/TPEL.2014.2357836.
[68] R. Technologies. "Evaporative Spray Cooling of High Power Electronics (HPE)." http://rinitech.com/wp-content/uploads/2016/01/EvapSprayCooling.pdf (accessed.
[69] H. Bostanci, D. V. Ee, B. A. Saarloos, D. P. Rini, and L. C. Chow, "Thermal Management of Power Inverter Modules at High Fluxes via Two-Phase Spray Cooling," *IEEE Transactions on Components, Packaging and Manufacturing Technology,* vol. 2, no. 9, pp. 1480-1485, 2012, doi: 10.1109/TCPMT.2012.2190933.
[70] R. Wang *et al.*, "A High-Temperature SiC Three-Phase AC - DC Converter Design for > 100/spl deg/C Ambient Temperature," *IEEE Transactions on Power Electronics,* vol. 28, no. 1, pp. 555-572, 2013, doi: 10.1109/TPEL.2012.2199131.
[71] P. Ning *et al.*, "High-Temperature Hardware: Development of a 10-kW High-Temperature, High-Power-Density Three-Phase ac-dc-ac SiC Converter," *IEEE Industrial Electronics Magazine,* vol. 7, no. 1, pp. 6-17, 2013, doi: 10.1109/MIE.2012.2231729.
[72] Y. Wu *et al.*, "Electrothermal-Control Co-Design of an All Silicon Carbide 2×250 kW Dual Inverter for Heavy-Duty Traction Applications," *IEEE Transactions on Industry Applications,* vol. 58, no. 1, pp. 505-516, 2022, doi: 10.1109/TIA.2021.3127144.
[73] D. B. N. Singh. "Silicon Carbide Inverter Development, Inverter Testing and Findings from Heavy-Duty Vehicle." https://www.psma.com/sites/default/files/IS14.3%20Silicon%20Carbide%20Inverter%20Development,%20Inverter%20Testing%20and%20Findings%20from%20Heavy-Duty%20Vehicle.pdf (accessed.
[74] M. A. A. Soles, "Silicon Carbide High Temperature and High Power Density Inverter Design," presented at the In Proceedings of the Ground Vehicle Systems Engineering and Technology Symposium (GVSETS), NDIA, Novi, MI, Aug. 13-15, 2019, 2019.
[75] J. Lu, Z. Zhou, J. Hao, Y. Hao, H. Zhang, and R. Hao, "High-temperature characteristics of SiC module and 100 kW SiC AC-DC converter at a junction temperature of 180 °C," *Global Energy Interconnection,* vol. 2, no. 6, pp. 521-530, 2019/12/01/ 2019, doi: https://doi.org/10.1016/j.gloei.2020.01.006.
[76] C. Zhang, S. Srdic, S. Lukic, Y. Kang, E. Choi, and E. Tafti, "A SiC-Based 100 kW High-Power-Density (34 kW/L) Electric Vehicle Traction Inverter," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 23-27 Sept. 2018 2018, pp. 3880-3885, doi: 10.1109/ECCE.2018.8558373.
[77] F. Qi, M. Wang, and L. Xu, "Investigation and Review of Challenges in a High-Temperature 30-kVA Three-Phase Inverter Using SiC MOSFETs," *IEEE Transactions on Industry Applications,* vol. 54, no. 3, pp. 2483-2491, 2018, doi: 10.1109/TIA.2018.2796059.
[78] K. Olejniczak *et al.*, "A compact 110 kVA, 140°C ambient, 105°C liquid cooled, all-SiC inverter for electric vehicle traction drives," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 26-30 March 2017 2017, pp. 735-742, doi: 10.1109/APEC.2017.7930776.
[79] M. R. Matthew Feurtado, Daniel Martin, Ty McNutt. (2019) Increasing Power Density In Three-Phase Inverters With Direct-Cooled SiC Power Modules. *How2Power*. Available: http://www.how2power.com/pdf_view.php?url=/newsletters/2010/articles/H2PToday2010_design_Wolfspeed.pdf
[80] F. Savi *et al.*, "High-Speed Electric Drives: A Step Towards System Design," *IEEE Open Journal of the Industrial Electronics Society,* vol. 1, pp. 10-21, 2020, doi: 10.1109/OJIES.2020.2973883.
[81] S. Wu, C. Tian, W. Zhao, J. Zhou, and X. Zhang, "Design and Analysis of an Integrated Modular Motor Drive for More Electric Aircraft," *IEEE Transactions on Transportation Electrification,* vol. 6, no. 4, pp. 1412-1420, 2020, doi: 10.1109/TTE.2020.2992901.

[82] R. Cuzner, D. Drews, and G. Venkataramanan, "Power Density and Efficiency Comparisons of System-Compatible Drive Topologies," *IEEE Transactions on Industry Applications,* vol. 51, no. 1, pp. 459-469, 2015, doi: 10.1109/TIA.2014.2334731.

[83] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Letters,* vol. 10, no. 10, pp. 455-457, 1989/10 1989, doi: 10.1109/55.43098.

[84] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations," *IEEE Transactions on Power Electronics,* vol. 29, no. 5, pp. 2393-2407, 2014, doi: 10.1109/TPEL.2013.2278919.

[85] W. Lee, S. Li, D. Han, B. Sarlioglu, T. A. Minav, and M. Pietola, "A Review of Integrated Motor Drive and Wide-Bandgap Power Electronics for High-Performance Electro-Hydrostatic Actuators," *IEEE Transactions on Transportation Electrification,* vol. 4, no. 3, pp. 684-693, 2018.

[86] A. Borghese *et al.*, "Statistical Analysis of the Electrothermal Imbalances of Mismatched Parallel SiC Power MOSFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 7, no. 3, pp. 1527-1538, 2019, doi: 10.1109/JESTPE.2019.2924735.

[87] T. Bertelshofer, A. Maerz, and M. Bakran, "Derating of Parallel SiC MOSFETs Considering Switching Imbalances," in *PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 5-7 June 2018 2018, pp. 1-8.

[88] J. Ke, Z. Zhao, P. Sun, H. Huang, J. Abuogo, and X. Cui, "Chips Classification for Suppressing Transient Current Imbalance of Parallel-Connected Silicon Carbide MOSFETs," *IEEE Transactions on Power Electronics,* vol. 35, no. 4, pp. 3963-3972, 2020, doi: 10.1109/TPEL.2019.2934739.

[89] J. Qu, Q. Zhang, X. Yuan, and S. Cui, "Design of a Paralleled SiC MOSFET Half-Bridge Unit With Distributed Arrangement of DC Capacitors," *IEEE Transactions on Power Electronics,* vol. 35, no. 10, pp. 10879-10891, 2020, doi: 10.1109/TPEL.2020.2978718.

[90] Q. Haihong *et al.*, "Influences of circuit mismatch on paralleling silicon carbide MOSFETs," in *2017 12th IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 18-20 June 2017 2017, pp. 556-561, doi: 10.1109/ICIEA.2017.8282906.

[91] P. A. Dahono, Y. Sato, and T. Kataoka, "Analysis and minimization of ripple components of input current and voltage of PWM inverters," *IEEE Transactions on Industry Applications,* vol. 32, no. 4, pp. 945-950, 1996, doi: 10.1109/28.511653.

[92] M. Vujacic, M. Hammami, M. Srndovic, and G. Grandi, "Evaluation of DC voltage ripple in three-phase PWM voltage source inverters," in *2017 IEEE 26th International Symposium on Industrial Electronics (ISIE)*, 19-21 June 2017 2017, pp. 711-716, doi: 10.1109/ISIE.2017.8001333.

[93] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," *IEEE Transactions on Industrial Electronics,* vol. 58, no. 7, pp. 2872-2882, 2011, doi: 10.1109/TIE.2010.2072896.

[94] Q. Xun, B. Xun, Z. Li, P. Wang, and Z. Cai, "Application of SiC power electronic devices in secondary power source for aircraft," *Renewable and Sustainable Energy Reviews,* vol. 70, pp. 1336-1342, 2017/04/01/ 2017, doi: https://doi.org/10.1016/j.rser.2016.12.035.

[95] M. Galea, P. Giangrande, V. Madonna, and G. Buticchi, "Reliability-Oriented Design of Electrical Machines: The Design Process for Machines' Insulation Systems MUST Evolve," *IEEE Industrial Electronics Magazine,* vol. 14, no. 1, pp. 20-28, 2020, doi: 10.1109/MIE.2019.2947688.

[96] S. Jahdi, O. Alatise, J. A. O. Gonzalez, R. Bonyadi, L. Ran, and P. Mawby, "Temperature and Switching Rate Dependence of Crosstalk in Si-IGBT and SiC Power Modules," *IEEE Transactions on Industrial Electronics,* vol. 63, no. 2, pp. 849-863, 2016, doi:

10.1109/TIE.2015.2491880.
[97] X. Long, Z. Jun, L. Pu, D. Chen, and W. Liang, "Analysis and Suppression of High Speed Dv/Dt Induced False Turn-on in GaN HEMT Phase-Leg Topology," *IEEE Access,* vol. 9, pp. 45259-45269, 2021, doi: 10.1109/ACCESS.2021.3066981.
[98] H. Li, Y. Jiang, Z. Qiu, Y. Wang, and Y. Ding, "A Predictive Algorithm for Crosstalk Peaks of SiC MOSFET by Considering the Nonlinearity of Gate-Drain Capacitance," *IEEE Transactions on Power Electronics,* vol. 36, no. 3, pp. 2823-2834, 2021, doi: 10.1109/TPEL.2020.3016155.
[99] K. Yamaguchi, J. Magome, and Y. Sasaki, "Fast and Low Loss Gate Driver for SiC-MOSFET," *Electronics and Communications in Japan,* https://doi.org/10.1002/ecj.11866 vol. 99, no. 10, pp. 13-23, 2016/10/01 2016, doi: https://doi.org/10.1002/ecj.11866.
[100] Y. Li, M. Liang, J. Chen, T. Q. Zheng, and H. Guo, "A Low Gate Turn-OFF Impedance Driver for Suppressing Crosstalk of SiC MOSFET Based on Different Discrete Packages," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 7, no. 1, pp. 353-365, 2019, doi: 10.1109/JESTPE.2018.2877968.
[101] H. Li *et al.*, "Assist Gate Driver Circuit on Crosstalk Suppression for SiC MOSFET Bridge Configuration," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 2, pp. 1611-1621, 2020, doi: 10.1109/JESTPE.2019.2914180.
[102] Z. Qiu *et al.*, "An Intelligent Three-level Active Gate Driver for Crosstalk Suppression of SiC MOSFET," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 11-15 Oct. 2020 2020, pp. 203-208, doi: 10.1109/ECCE44975.2020.9236368.
[103] H. Li, Y. Jiang, Z. Qiu, T. Shao, and Y. Wang, "A Multi-step Active Gate Driver for Suppressing Crosstalk of SiC MOSFET," in *2020 IEEE 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, 29 Nov.-2 Dec. 2020 2020, pp. 1868-1873, doi: 10.1109/IPEMC-ECCEAsia48364.2020.9367746.
[104] "Semiconductor Components Industries, "MOSFET - SiC Power, Single N-Channel, D2PAK-7L 1200 V, 20 mOhm, 98 A", NVBG020N120SC1 datasheet " 2018 [revised June 2021].
[105] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active Gate Driver for Crosstalk Suppression of SiC Devices in a Phase-Leg Configuration," *IEEE Transactions on Power Electronics,* vol. 29, no. 4, pp. 1986-1997, 2014, doi: 10.1109/TPEL.2013.2268058.
[106] S. Lineykin and S. Ben-Yaakov, "Modeling and Analysis of Thermoelectric Modules," *IEEE Transactions on Industry Applications,* vol. 43, no. 2, pp. 505-512, 2007, doi: 10.1109/TIA.2006.889813.
[107] J. J. Wolmarans, M. B. Gerber, H. Polinder, S. W. H. d. Haan, J. A. Ferreira, and D. Clarenbach, "A 50kW integrated fault tolerant permanent magnet machine and motor drive," in *2008 IEEE Power Electronics Specialists Conference*, 15-19 June 2008 2008, pp. 345-351, doi: 10.1109/PESC.2008.4591953.
[108] A. Tenconi, F. Profumo, S. E. Bauer, and M. D. Hennen, "Temperatures Evaluation in an Integrated Motor Drive for Traction Applications," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 10, pp. 3619-3626, 2008, doi: 10.1109/TIE.2008.2003099.
[109] M. D. Hennen, M. Niessen, C. Heyers, H. J. Brauer, and R. W. D. Doncker, "Development and Control of an Integrated and Distributed Inverter for a Fault Tolerant Five-Phase Switched Reluctance Traction Drive," *IEEE Transactions on Power Electronics,* vol. 27, no. 2, pp. 547-554, 2012, doi: 10.1109/TPEL.2011.2132763.
[110] Y. Burkhardt, A. Spagnolo, P. Lucas, M. Zavesky, and P. Brockerhoff, "Design and analysis of a highly integrated 9-phase drivetrain for EV applications," in *2014 International Conference on Electrical Machines (ICEM)*, 2-5 Sept. 2014 2014, pp. 450-456, doi: 10.1109/ICELMACH.2014.6960219.
[111] J. Hemsen *et al.*, "Innovative and highly integrated modular electric drivetrain," *World Electric Vehicle Journal,* vol. 10, no. 4, p. 89, 2019.
[112] X. Zhong, X. Wu, W. Zhou, and K. Sheng, "An All-SiC High-Frequency Boost DC–DC Converter Operating at 320 °C Junction Temperature," *IEEE Transactions on Power*

Electronics, vol. 29, no. 10, pp. 5091-5096, 2014, doi: 10.1109/TPEL.2014.2311800.

[113] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications," *IEEE Transactions on Power Electronics,* vol. 29, no. 5, pp. 2307-2320, 2014, doi: 10.1109/TPEL.2013.2283245.

Appendix A

Lists of IMD and HT power electronics

Table A1– IMD at simulation stage of development (“concept”)

IMD type	PE location	Power, kW	Material	Power switch	Application	Year	Ref.
ISMD(PE)	ERS	50				2008	[107]
IMD	ETS	24				2008	[108]
IMD	EAEp	160	Si	custom HB module	EV	2010	[52]
IMMD	EAEp	0,8		MOSFET		2013	[22]
ISMD(PE)	EAEp	290	SiC	custom HB module	EV	2014	[53]
ISMD(PE)	EAEp	80	SiC	custom module		2018	[42]
IMD	EAEp	110				2020	[81]

Table A2 –IMD with reported prototypes and test results (“prototypes”)

IMD type	PE location	Power, kW	Material	Power switch	Application	kW/kg	kW/L	Year	Ref.
ISMD(PE)	IAEp	30	Si	Custom module				2005	[25]
IMD	ERS	100	Si	custom HB module	EV			2006	[26]
ISMD(PE)	EAEp	67						2012	[109]
IMD	EAEp	55	Si	custom module		15,6	17,8	2013	[49]
IMD	EAEp	10.5						2014	[50]
IMMD	EAEp	18	Si	TO-247 IGBT				2014	[24]
IMD	EAEp	55	Si	commercial module	EV (Motor Brain)	0,7*		2014	[110]
IMD	EAEp	2	GaN	EPC2018				2015	[43]
ISMD(PE)	EAEp	35	Si	IPB065N15N3G				2017	[47]
ISMD(EM)	EAEp	38	SiC	C2M0040120D				2018	[48]
IMD	ETS	157	GaN	custom module	EV (ModulED)			2019	[111]
ISMD(PE)	EAEp	40	SiC	custom HB module	in-wheel	1,1**		2020	[10]
IMMD	EAEp	20	Si					2020	[23]
ISMD(PE)	ERS	200	SiC		Aero (H3X)	13,3*	26*	2020	[34]
IMD	ICEp	1	GaN	MOSFET	UAF			2021	[40]
IMMD	ERS	17	GaN	GS66508B				2021	[46]

* - includes an inverter and a motor; ** - includes a motor, an inverter and a gear.

Table A3 - Commercially available (OEM or as a part of a system) IMD

IMD type	PE location	Power, kW	Material	Power switch	Application	kW/kg	kW/L	Year	Ref.
IMD	ETS	80	Si	custom 3ph module	Nissan Leaf	5,22	6,1	2012	[14]
IMD	EAEp	310	Si	TO-247	Tesla Model S 2015	-	≈20	2012	[51]
IMD	ETS	180	Si	custom HB module	Chev VOLT 2gen	17,3	21,7	2015	[55]
IMD	ETS	215	Si		Cadillac CT6	16,5	23	2016	[57]
IMD	ETS	125	Si	FS800R07A2E3	BMW i3	6,6	-	2016	[54]
IMD	ETS	160	Si	custom HB module	Toyota 4th gen	13,4	23,7	2016	[56]
IMD	ETEp	210	SiC	custom MOSFET	Tesla Model 3	43,6		2017	[51]
IMD	EAEp	32	Si	MOSFET	EV (IPM 278 LV)	2,6*		2018	[29]
IMD	ETS	160			BorgWarner iDM	-	-	2019	[31]
IMD	ETS	160	Si	custom HB module	Audi E-tron S 2019	19,6	2	2019	[58]
IMD	ETS	150			EV(Ni150Ex)	1,7**		2019	[30]
IMD	EAEp	400	SiC		EV (CTU400)	4,4**	9.5**	2020	[28]
IMD	ETS	100			EV(Ni100Ex)	1,8**		2020	[30]
IMD	ETS	70			EV(Ni70Ex)	1,4**		2021	[30]
IMD	ETS	200			EV(Ni200Ex)	2,1**		2023	[30]

* - includes an inverter and a motor; ** - includes a motor, an inverter and a gear.

Table A4 – Examples of HT power electronics

Application	Material	Power switch	Temperature, ℃		Cooling type	Details	Year	Ref
			Ambient/ Coolant	Junction tested				
Inverter	SiC	CAS325M12HM2	-/100	140	Indirect, pin fin	2*250kW	2022	[72]
EV	SiC	CAS325M12HM2	-/115	-	Indirect	200kW	2019	[73]
EV	SiC		-/105		Indirect	175kW	2019	[74]
Inverter	SiC	CAS300M12BM2	-	186	Heatsink, air	100kW	2019	[75]
Inverter	SiC	CAS325M12HM2	105/65	-	Indirect, pin fin	100kW	2018	[76]
Inverter	SiC	CAS300M12BM2	180/50	90	Indirect	31kVA	2018	[77]
Inverter	SiC	CAS325M12HM2	140/105	-	Indirect	30kW	2018	[78]
DC-DC	SiC	Custom MOSFET	-	320	-	-	2014	[112]
Inverter	SiC	TO-247	120/-	175	Heatsink, air	10kW	2014	[19]
Inverter	SiC	Custom 3ph module	-	200	-	1200V,60A MOSFETs	2014	[113]
AC-DC	SiC	Custom module	150/127	227	Heatsink, air		2013	[70]
AC-AC	SiC	Custom module	25/130	222	Heatsink, air	10kW	2013	[71]
IMD	Si	IGBT HB 150A 650V	-/105	120*	Indirect	55kW	2013	[49]
EV	Si	SKAI 4001GD06	-/100	125	Direct, spray (2 ph)	250kW	2007	[68]
IMD	Si	Custom module	-/115		Direct	100kW	2006	[26]

List of Acronyms

BJT - Bipolar Junction Transistor
CM – common mode’
DC – direct current
EM – electrical machine
EMI – electro-magnetic interference
ESR – equivalent serial resistance
EV – electric vehicle
EDU - electric drive unit
GaN - Gallium nitride
GD – gate driver
GHG - Greenhouse gas
GPM – gallon per minute
HB – half-bridge
HEV - hybrid electric vehicle
HS/LS – high side/low side
HT – high temperature
HTC – heat transfer coefficient
HV – high voltage
HVAC - heating, ventilation, and air conditioning
ICE - Internal combustion engine
ICEV - Internal combustion engine vehicle
IGBT - insulated-gate bipolar transistor
IMD - integrated motor drive
IMMD - Integrated modular motor drive
ISMD - Integrated semi-modular motor drive
MOSFET - Metal Oxide Silicon Field Effect Transistor
NTC – negative temperature coefficient
OEM - original equipment manufacturer
PCB – printed circuit board
PE – power electronics
PMSM – Permanent Magnet Synchronous Motor
PTC – positive temperature coefficient
SiC - silicon carbide
TIM – thermal interface material
UAV - unmanned aerial vehicle
VBBSC – Voltage back-to-back source converter
WBG – wide band gap
SMT - surface mount technology
SMD - surface mount device
IMS – insulated metal substrate
DBC - Direct Copper Bonding
THT - through-hole technology

DSC - double side cooling
FEA – finite-element analysis
VSI - Voltage Source Inverter
THD - Total Harmonic Distortion
CSI - Current source inverters

List of Symbols

$\Delta v_{R\,PP}$ – DC-link voltage ripples
ΔV_{TH} – deviation of MOSFET threshold voltage
A_{CS} – area of CS housing
A_{HS} – area of component's thermal pad
A_{SMT} – total area occupied by SMT power switches
A_{THT} – total area occupied by THT power switches
C_{DC} – Capacitance of inverter's DC-link capacitor
C_{GD} – gate-drain MOSFET capacitance
C_{ISS} – input capacitance of a MOSFET
C_{rss} or C_{gd} – reverse transfer capacitance
$E_{SW\,T\,RATED}$ – total switching loss energy at rated conditions
F_{SW} – switching frequency
h_{CP} – heat transfer coefficient of a cold plate
h_{j-c} – junction-coolant transfer coefficient
$H_{MOSFETs}$ – height of a power board
H_{PE1} – height of supplementary PE part
$I_{C\,RMS}$ – RMS current of DC-link capacitor
I_{CS} – current of secondary coil
$I_{D\,MAX\,RMS}$ - maximum RMS drain current of a device
$I_{D\,RATED}$ - RMS drain current of a device at rated conditions
$I_{dc\,max}$ – maximum continuous current of a device
I_{dg} – drain-gate current
$I_{ds\,RMS\,G}$ – RMS drain current of MOSFET group
$I_{ds\,RMS}$ – RMS drain current of a single device
I_{ds} – drain current of a single device
$I_{G\,Miller}$ – gate current at Miller's plateau
I_{Gk} – gate current of k-MOSFET in the group
I_{GTotal} – gate current of a MOSFET group
$I_{GtotalMAX}$ – maximum output current of a gate driver
I_{idle} – current of sensor's power supply
I_{M} – TEM input current
$I_{PH\,MAX}$ - maximum of phase current
K_I – drain current scaling coefficient
KR_{T_J} – junction temperature scaling coefficient of active channel resistance
K_{Rg} – gate resistance scaling coefficient
KR_I – drain current scaling coefficient of active channel resistance
K_{Tj} – junction temperature scaling coefficient
K_{Vdc} – DC-link voltage scaling coefficient
L_{ACTIVE} – length of EM stator
L_{EW} – length of EM front endwinding

L_{PCB} – length of the PCB with power switches (square shape)
L_{SEW} - length of EM back endwinding
N_{PPG} – number of MOSFETs per a group
OD_S – outer diameter of the stator
P_{BJT} - power losses of BJTs
P_C - MOSFET's conduction power losses
P_{coil} - inductor active losses
P_{COLD} - power being pumped from the cold side
$P_{CS\,total}$ – total power losses of current sensor
P_{Hall} - power losses of Hall supply
P_{HOT} – power dissipated through the hot side of TEM
$P_{LEAK\,W}$ – heat transferring from primary conductor to the case of CS
P_{LEAK} – heat transferring from environmental to the case of CS
P_{LOSSES} – total losses of an inverter
P_{MOSFET} –MOSFET's total power losses
P_{OUT} – output power of an inverter
P_{SW} - MOSFET's switching power losses
Q_g – total gate charge
Q_{gd} – drain-gate charge
R_{coil} – resistance of the sensor's secondary side coil
$R_{DS\,ON}$ – active resistance of turned-on MOSFET's channel
$R_{DS\,ON25}$ - active resistance of turned-on MOSFET's channel at T_j =25°C
$R_{g\,ext}$ – external gate resistance
$R_{g\,inner}$ – inner gate resistance
R_{meas} – measuring resistance
$Rn_{ds\,on\,TjHT}$ - normalized value of drain-source channel resistance
R_{PCB} –radius of the PCB with power switches (round shape)
R_{TEM} – TEM active resistance
$S_{PCB\,AREA}$ – heat transferring area of a PCB
T_{AMB} – ambient temperature
T_{BASE} – temperature of the aluminium base
$T_{CASE\,C}$ – temperature of CS case (calculated)
T_{CASE} – temperature of CS case
T_{COLD} – temperature of the TEM's cold side
T_{COLD} – temperature of the TEM's cold side
$T_{COOLANT}$ – coolant temperature
$T_{HOT\,C}$ – temperature of the TEM's hot side (calculated)
T_{HOT} – temperature of the TEM's hot side
T_{HtS} – CS heat sink temperature
$T_{j\,MAX}$ – maximum value of junction temperature for a device
T_j – junction temperature
T_{jHT} – second temperature point for $R_{DS\,ON}$ temperature approximation

T_{jLT} – maximum junction temperature where $Rn_{ds\ on\ Tj}$ is equal to 1

t_{rise} - rise time of drain-source voltage

$T_{SW\ EXP}$ – expected duration of drain-source voltage's transition

T_{SW} – duration of drain-source voltage's transition

$V_{DC\ MAX}$ - maximum drain-source DC voltage of a switch

$V_{DCrated}$ – drain-source DC voltage at rated conditions

V_{GDMax} – maximum gate driver voltage

V_{GDMill} – voltage of Miller's plateau

V_{GDMin} – minimum gate driver voltage

V_{Gk} – gate–source voltage of k-MOSFET in the group

V_M – TEM input voltage

V_{PH} – phase voltage

V_{TH} – MOSFET threshold voltage

W_{module} – weight of power switches (power modules)

W_{PCB} – width of the PCB with power switches (square shape)

W_{SMT} – weight of power board (SMT MOSFETs)

Θ_{CASE} - thermal resistance of CS case

Θ_{C-hs} – case-heat sink thermal resistance

$\theta_{IND\ HS}$ – thermal resistance between the secondary coil and the heat sink

$\theta_{J\ HS}$ - thermal resistance between the BJT and the heat sink

Θ_{J-Amb} – junction-ambient thermal resistance

Θ_{J-C} – junction-case thermal resistance

Θ_M - hot-to-cold sides thermal resistance

$\Theta_{Pre\ pad}$ – Prepreg thermal resistance (area under the thermal pad)

Θ_{TIM} – thermal resistance of TIM

ω_F – angular fundamental frequency

$\mathcal{T}_{COLDPLATE}$ – thickness of a IMD cold plate

$\mathcal{T}_{FP}$ - thickness of EM front plate

$\mathcal{T}_{WALL}$ – thickness of PE and EM housings

$\mathcal{V}_{EM}$ – volume of a IMD machine

$\mathcal{V}_{inv}$ – volume of an IMD inverter

FOM – figure of merit

M – modulation index [0;1]

φ – phase angle